

COMPAL CONFIDENTIAL

MODEL NAME : Loki15/17

PCB NO : DA8001BS000

BOM P/N : 431A7Y31L01

KBL-U+MEC1416 board 2017-07-28

REV : 1.0 (A00)

PCB R1	PCB R3
ZZZ  DA8001BS000 PCB@ PCB 21C LA-F115P REV0 M/B 3	ZZZ  DAZ21C00101 PCB_R3@ PCB CAL50 LA-F115P LS-F111P GOLD A31 !
KBL R1	KBL R3
UC1  SA0000AWC0L I7KBLR_1.8G_QS@ S IC A31 FJ8067703281816 QNBF Y0 1.8G	UC1  SA0000AWC2L I7KBLR_R3@ S IC FJ8067703281816 SR3LC Y0 1.8G A31!
UC1  SA0000A370L I5KBLU_2.5G_R1@ S IC FJ8067702739739 SR2ZU H0 2.5G A31!	UC1  SA0000AWB3L I5KBLR_R3@ S IC FJ8067703282221 SR3LB Y0 1.6G A31!
UC1  SA0000AWB1L I5KBLR_1.6G_QS@ S IC A31 FJ8067703282221 QNEG Y0 1.6G	UC1  SA0000B2Y1L I3KBLU_R3@ S IC FJ8067702739765 SR3JY H0 2.7G A31!
UC1  SA0000AQZ0L I7KBLR_1.8G_ES@ S IC A31 FJ8067703281813 QN5C Y0 1.8G	UC1  SA0000ADV3L KBLU_Pentium_R3@ S IC FJ8067702739932 SR348 H0 2.3G A31!
UC1  SA0000A344L I7KBLU_2.7G@ S IC FJ8067702739740 SR2ZV H0 2.7G A31!	UC1  SA0000ADL3L KBLU_Celeron_R3@ S IC FJ8067702739933 SR349 H0 1.8G A31!
UC1  SA0000ACL0L I3SKL_2.0G_SMB0@ S IC FJ8066201931106 SR2UW D1 2G A31!	UC1  SA0000ACL1L I3SKL_SMB0_R3@ S IC FJ8066201931106 SR2UW D1 2G A31!

@ : Un-pop Component
UMA@/DIS@ : UMA & DIS Type
U22@/U42@ : KBL U/KBL U-R
SKL@/KBL@:SKL/KBL
EC@ : EC
JP@/PJP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
TYPEC@EMI@/TYPEC@ESD@/TYPEC@RF@:EMI, ESD ,RFTYPEC Component
MAD@RF@:RF MAD Component
LOKI@EMI@/LOKI@ESD@:EMI/ESD LOKI Component
CMC@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
TPM@/FTPM@ : HW TPM/SW TPM
MMC@ : eMMC
FFS@ : Free Fall Sensor
TYPEC@/LOKI@TYPEC@ : typeC
DSX@ : Deep sleep
GEN8@/GEN9@:RTC GEN8/9
ODD@:ODD Component
FP@:Finger Printer

M2_50@ : GPU R17M_2_50
2G@/2G_H@/2G_S@/2G_M@ : VRAM type
4G@/4G_H@/4G_S@/4G_M@ : VRAM type

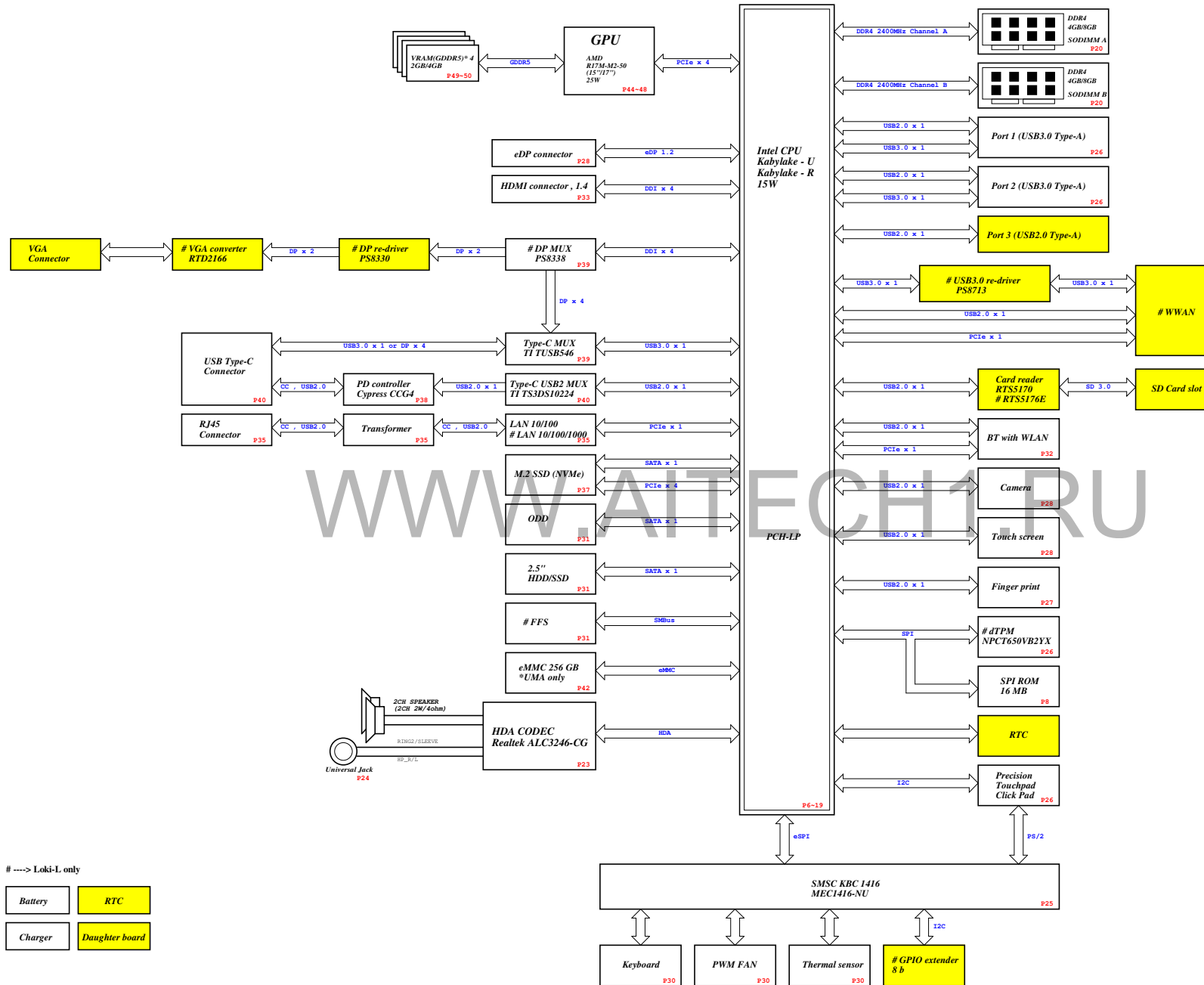
Layout Dell logo



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REV: X00
PWB: 9HTP8

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Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title	Cover Page
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Loki/Loki-L Block Diagram



Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	LOW	HIGH	HIGH	ON	ON	OFF	OFF

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 port3, IO/B
3	USB2.0 Port2
4	TypeC
5	Camera
6	Card reader , IO/B
7	BT
8	Touch screen
9	Finger printer
10	WWAN , IO/B

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1			USB3.0 port1
USB3.0-2			WWAN , IO/B
USB3.0-3			USB3.0 port2
USB3.0-4			TypeC
USB3.0-5	PCIE-1		GPU
USB3.0-6	PCIE-2		GPU
	PCIE-3		GPU
	PCIE-4		GPU
	PCIE-5		10/100 LAN
	PCIE-6		WLAN
	PCIE-7	SATA-0	SATA HDD
	PCIE-8	SATA-1	SATA ODD
	PCIE-9		NVME SSD
	PCIE-10		NVME SSD
	PCIE-11	SATA-1*	NVME SSD
	PCIE-12	SATA-2	NVME SSD

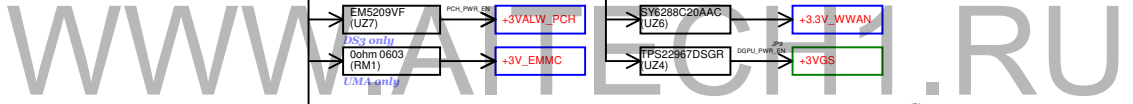
Power Plane	Description	S0	S3	DS3	S4/S5	M3
+SDC_IN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+1.0V_PRIM	System +1.0V power rail	ON	ON	OFF	ON*	ON
+1.0VS_VCCIO	+1.0VS IO power rail	ON	OFF	OFF	OFF	OFF
+1.0V_MPHYPLL	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	OFF	ON/OFF	ON
+0.95VSDGPU	+0.9VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.35V_MEM_GFX	+1.35VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.2V_DDR	DDR4/L-RS +1.2V power rail	ON	ON	ON	OFF	ON
+2.5V_MEM	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF	ON
+1.8V_PRIM	System +1.8V power rail	ON	ON	OFF	ON*	ON
+1.8VS	System +1.8VS power rail	ON	OFF	OFF	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3.3V_ALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	OFF	ON*	ON
+3VS	System +3VS power rail	ON	OFF	OFF	OFF	ON
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	ON
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	OFF	OFF	OFF	ON
+RTC_CELL	RTC power	ON	ON	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF	ON

High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
USB3 #1 (capable of OTG)	USB3 #2	USB3 #3	USB3 #4	USB3 #5	USB3 #6	PCIe #3	PCIe #4	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12
					PCIe #1						SATA #1A			SATA #1B	SATA #2
							GPIO	GPIO			SATA #0		GPIO		
								GPIO							
						X4			X4				X4		
					X2	X2		X2	X2	X2				X2	
								Intel® RST for PCIe Storage						Intel® RST for PCIe Storage	

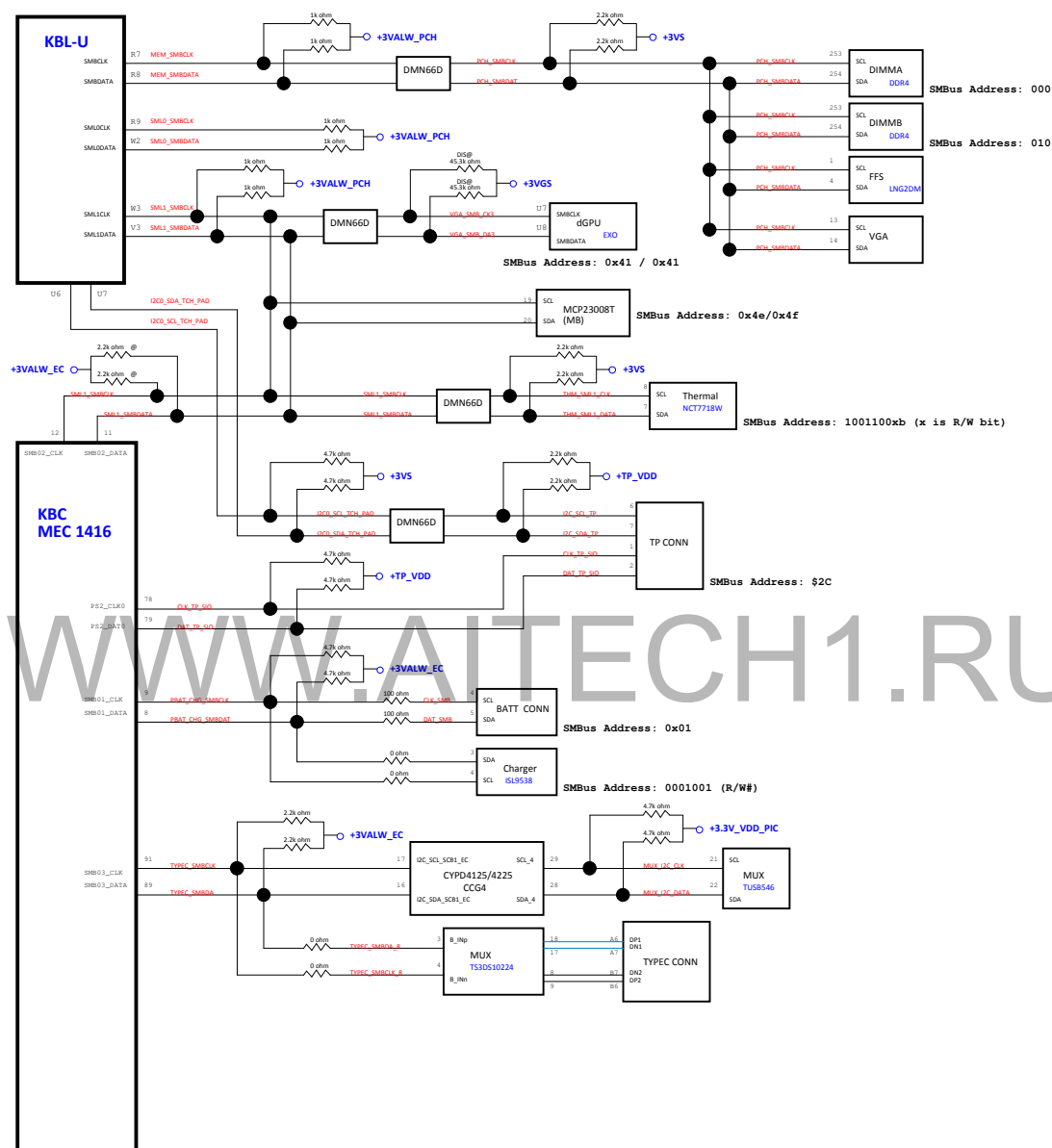
Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT
2	100	13.7	2.902	
3	100	17.8	2.801	DVT1
4	100	22.1	2.703	
5	100	27.0	2.598	DVT2
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	Pilot
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	
15	100	120.0	1.500	
16	100	137.0	1.392	
17	100	154.0	1.299	
18	100	200.0	1.100	
19	100	232.0	0.994	

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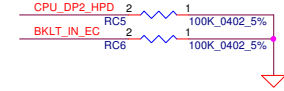
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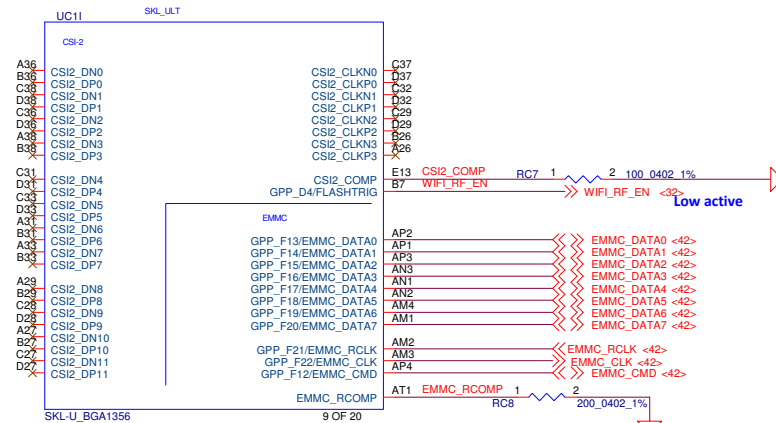
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SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0

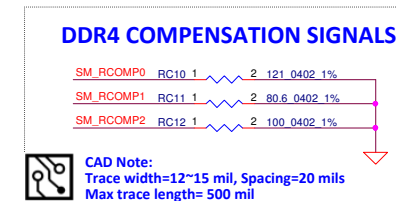
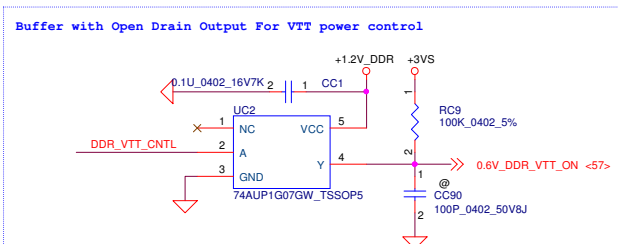
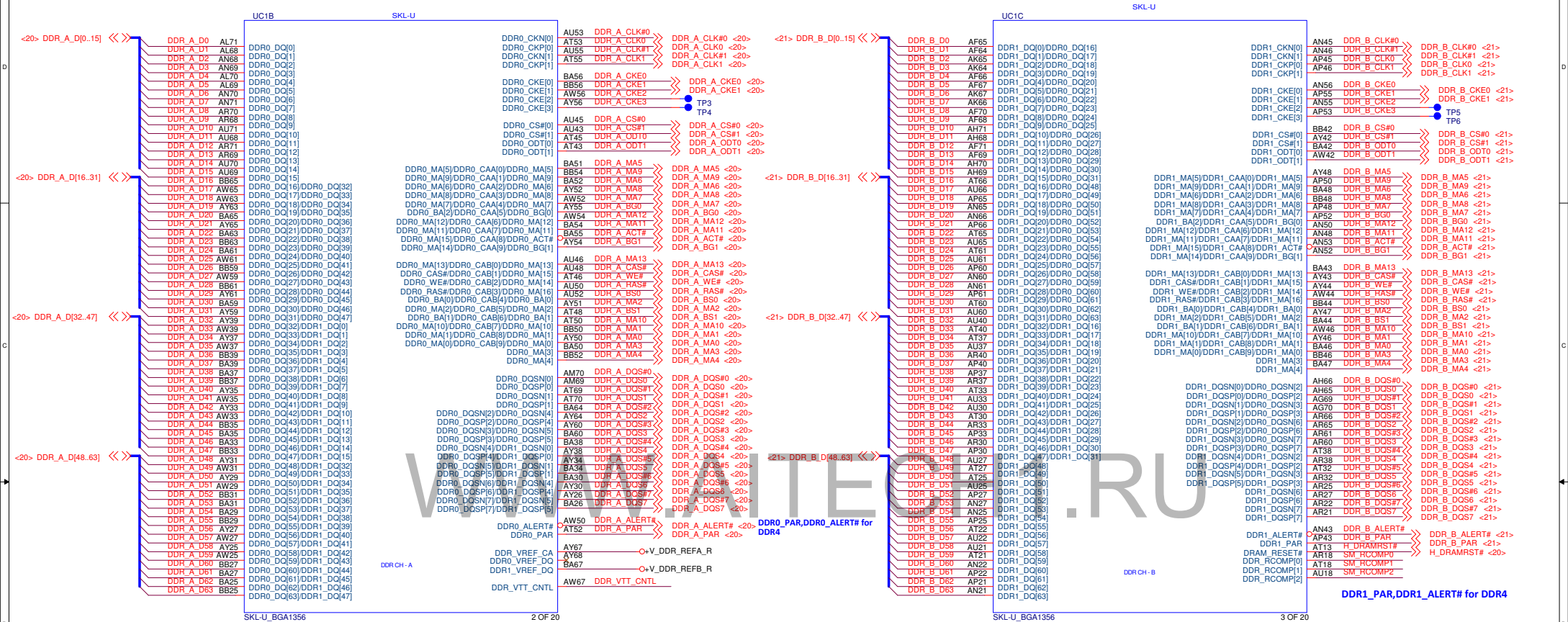


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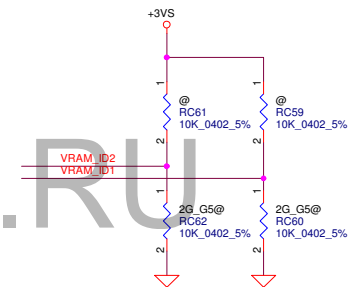
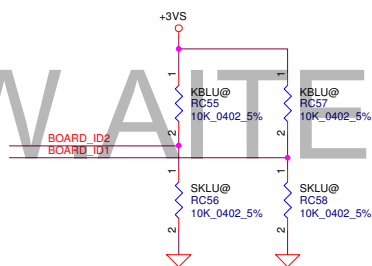
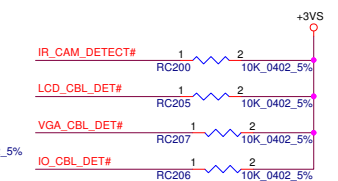
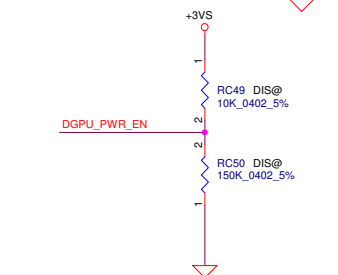
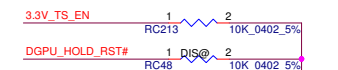
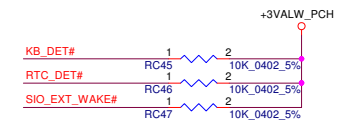
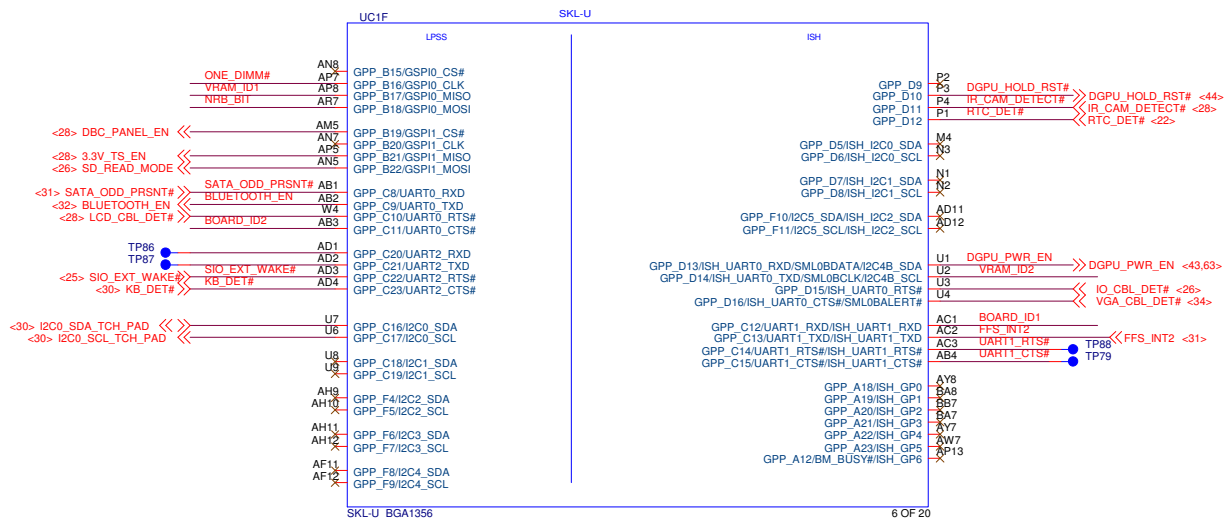
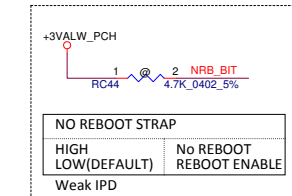
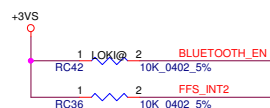
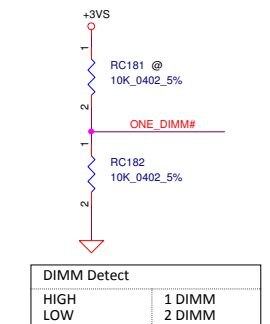
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DDR4 Interleaved Memory



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Main Func = CPU



CPU ID (PCBA VRAM Size Config.)	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
KBL-U	1	1
KBL-R	1	0
Reserved	0	1
SKL-U	0	0

RC55 KBLR@ 10K_0402_5% SD028100280

RC58 KBLR@ 10K_0402_5% SD028100280

VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_D14)	VBIOS_ID1 (GPP_B17)
2G GDDR5	0	0
4G GDDR5	0	1
Reserved	1	0
Reserved	1	1

RC62 4G_G5@ 10K_0402_5% SD028100280

RC59 4G_G5@ 10K_0402_5% SD028100280

Main Func = CPU

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GPU ---->

LOM ---->

WLAN ---->

SATA HDD ---->

SATA ODD ---->

PCIe SSD ---->

PCIe SSD ---->

PEG_GTX_C_HRX_P0 H13
PEG_GTX_C_HRX_N0 G13
PEG_HTX_C_GRX_P0 B17
PEG_HTX_C_GRX_N0 A17
PEG_GTX_C_HRX_P1 G11
PEG_GTX_C_HRX_N1 F11
PEG_HTX_C_GRX_P1 D16
PEG_HTX_C_GRX_N1 C16
PEG_GTX_C_HRX_P2 H16
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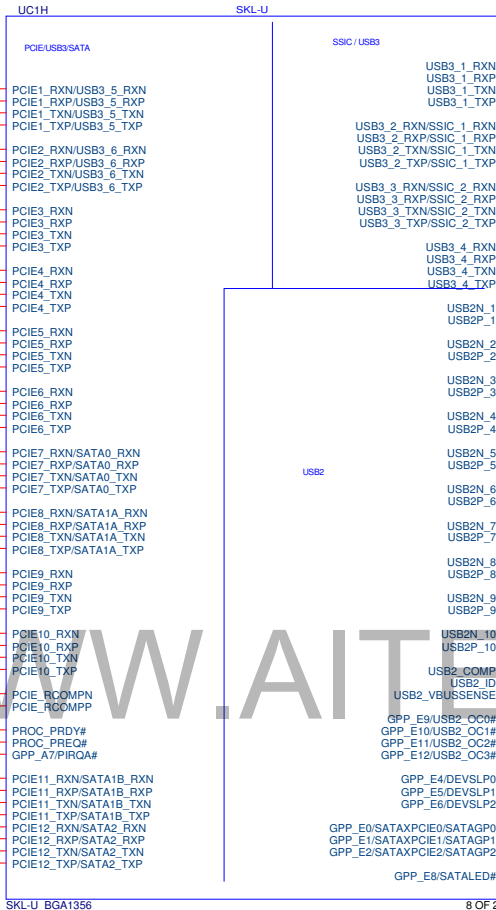
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PCIE_R0COMP# D5
PCIE_R0COMP# C5

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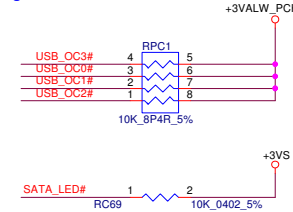
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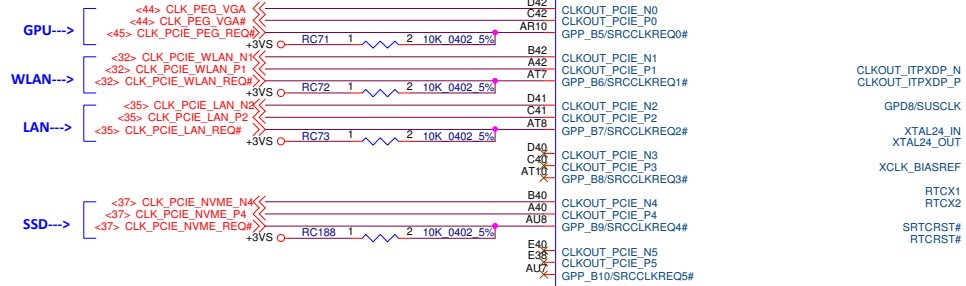
COMPENSATION PD FOR USBCOMP

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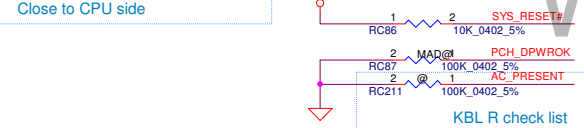
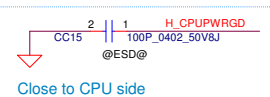
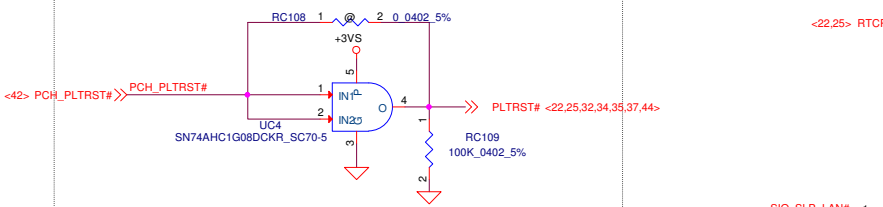


GPIO	Device Control
USB_OC0#	USB Port 1
USB_OC1#	WWAN
USB_OC2#	USB Port 4 (Type-C)
USB_OC3#	NA

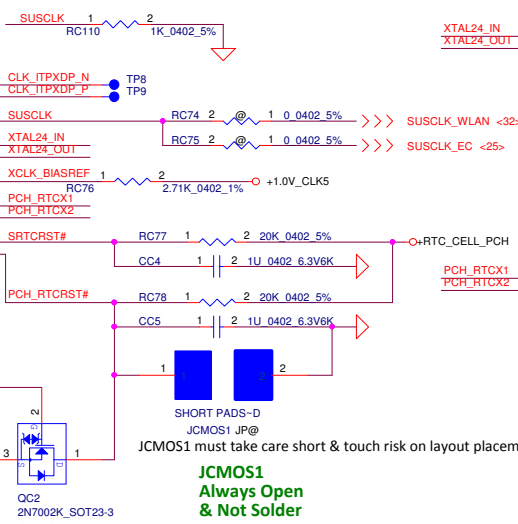
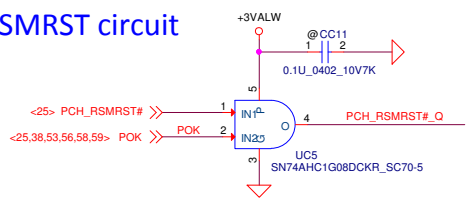
Main Func = CPU



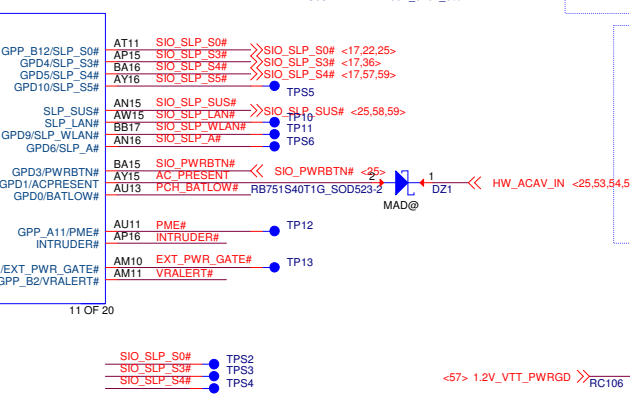
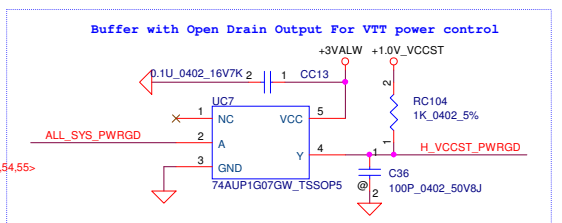
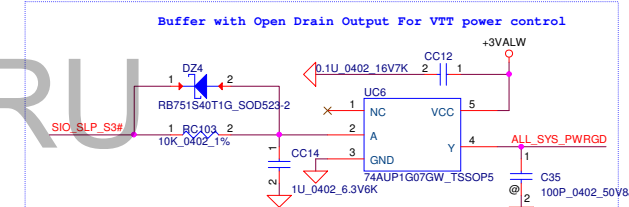
PCH_PLTRST#



RSMRST circuit

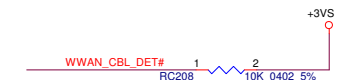
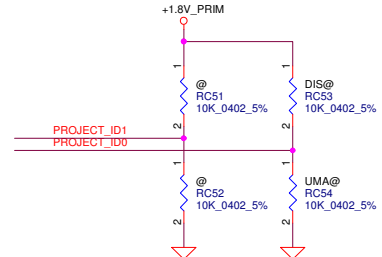
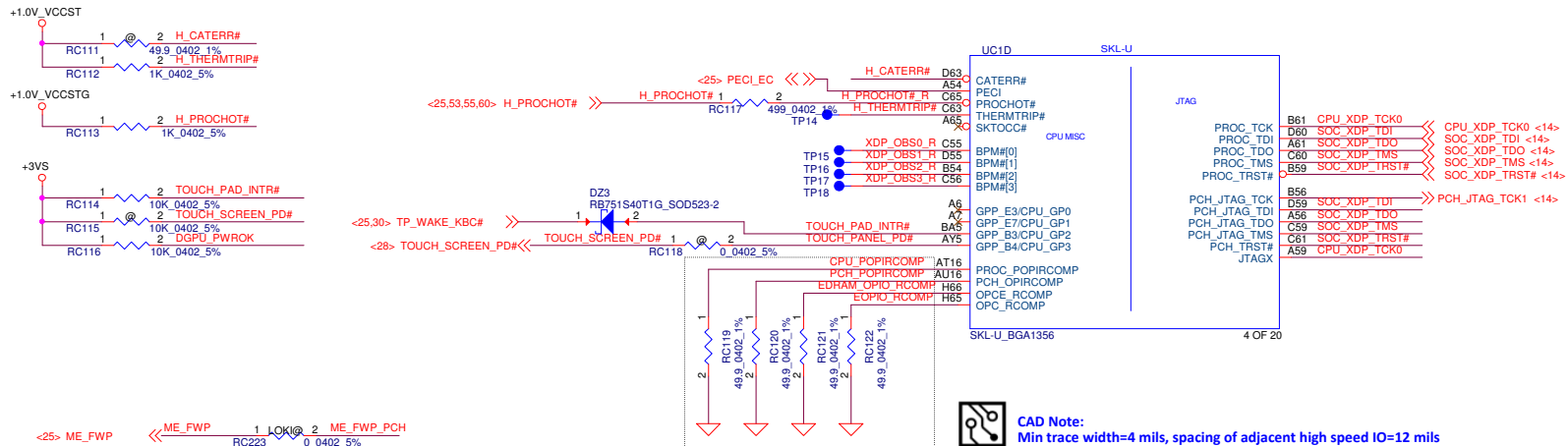


JCMOS1 Always Open & Not Solder



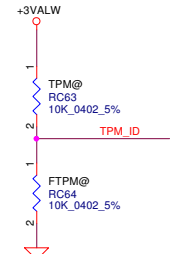
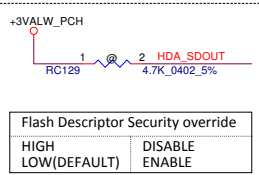
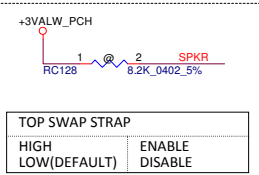
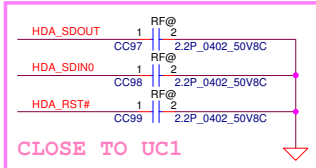
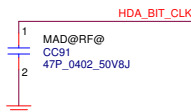
Security Classification	Compal Secret Data		Title	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	2017/12/01
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MCP(6/14)CLK,PM,RTC				LA-F115P
Date: Friday, July 28, 2017				Sheet 11 of 65

Main Func = CPU



ME_FWP

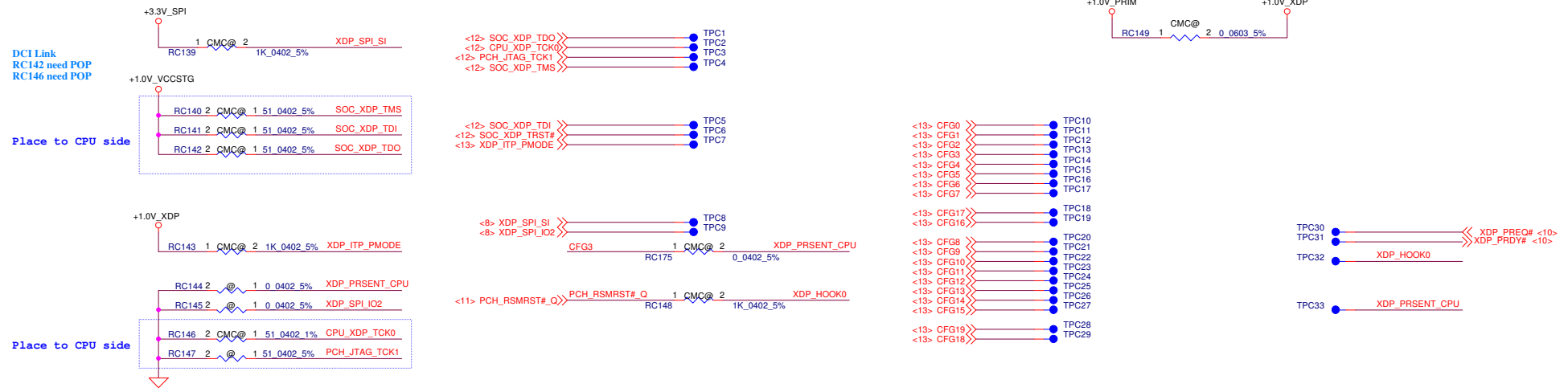
- LOW = ENABLE -->ME lock, can't update ME
- HIGH = DISABLE -->ME un-lock, can update ME



Security Classification		Compal Secret Data		Title	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	MCP(7/14)MISC, JTAG, HDA, SDIO	
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				LA-F115P	0.1
Date: Friday, July 28, 2017		Sheet 12 of 65			

Connector Less Routing Topology

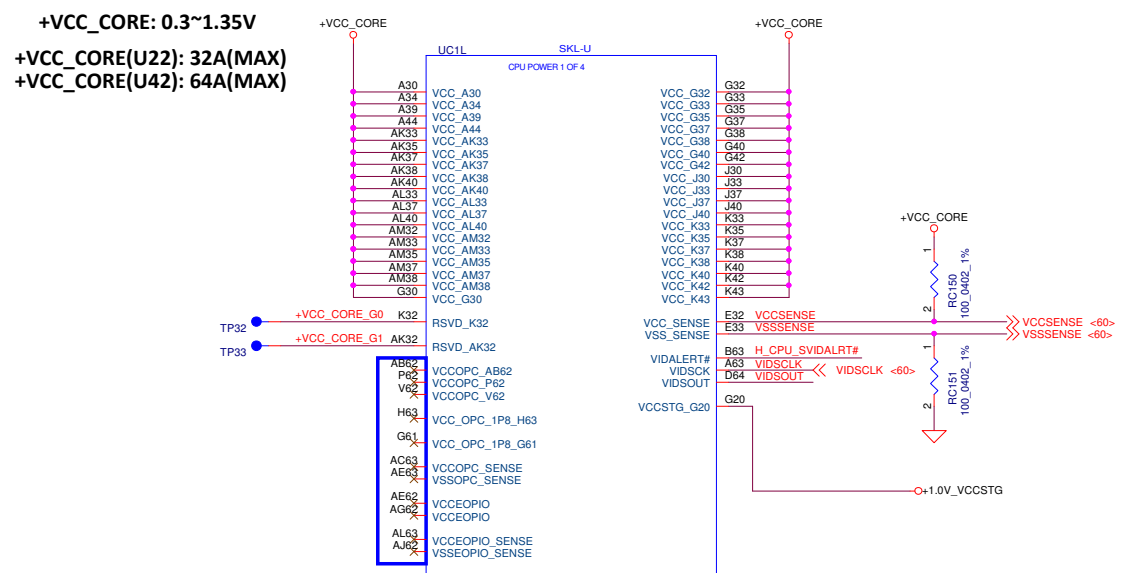
PRIMARY CMC CONN



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Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2016/12/01		Deciphered Date		2017/12/01		Title	
								MCP(9/14)XDP	
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						LA-F115P		0.1	
						Date:		Friday, July 28, 2017	
						Sheet		14 of 65	

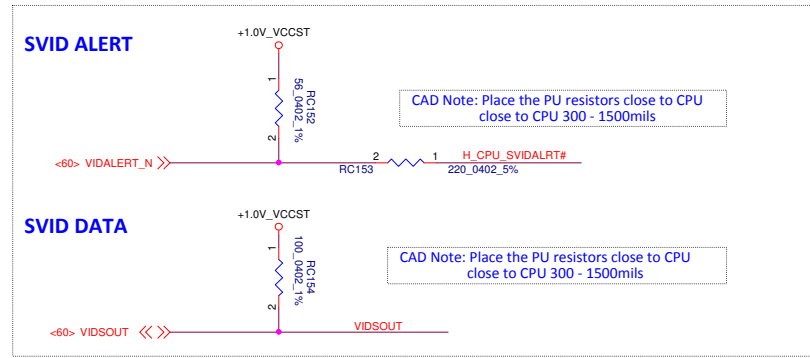
Main Func = CPU



PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Power caps > Power source

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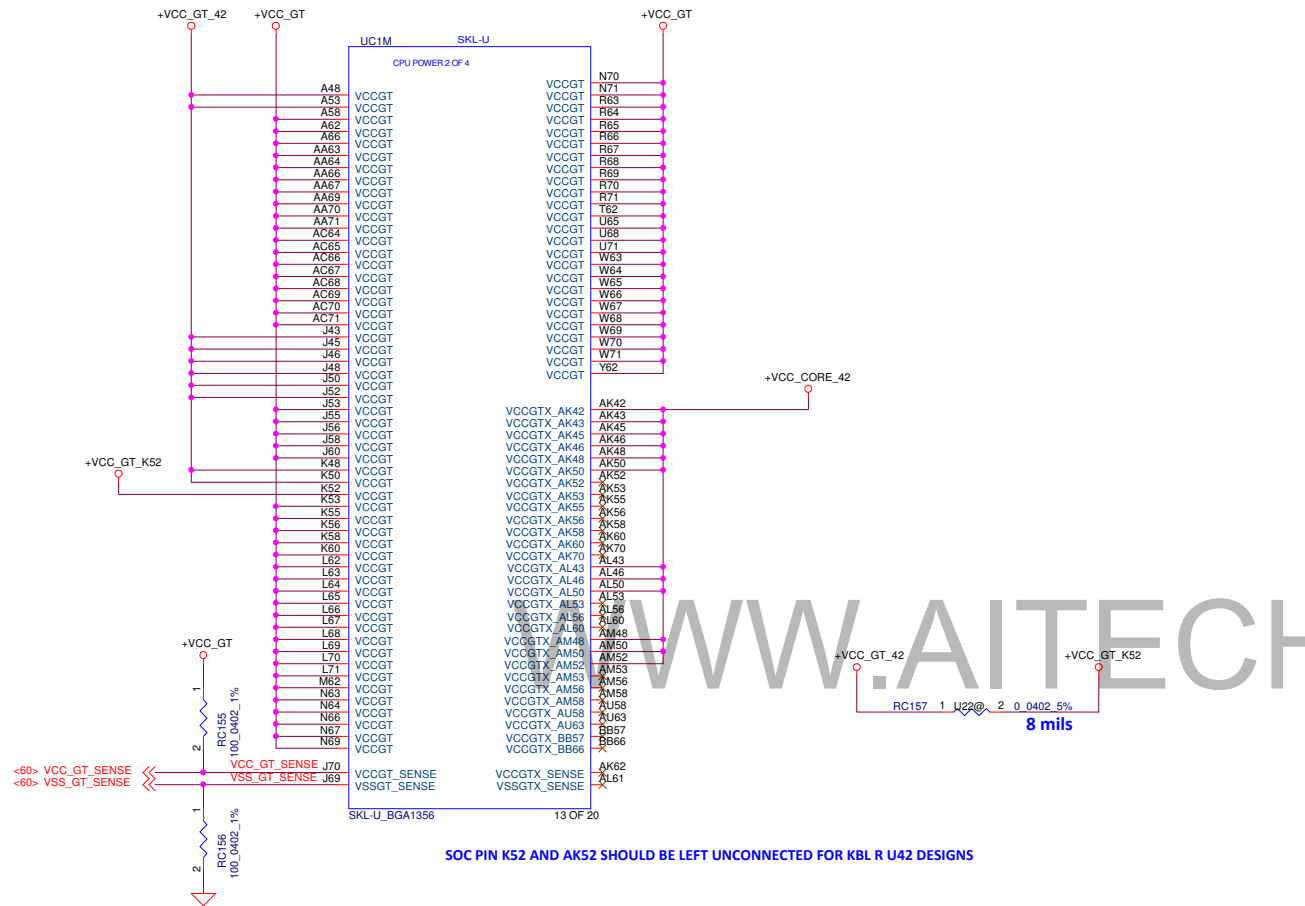


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title	MCP(10/14)PWR-VCC CORE
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				Date	Friday, July 28, 2017
				Sheet	15 of 65
				Rev	0.1

Main Func = CPU

+VCCGT: 0.3~1.35V
+VCCGTX: 0.3~1.35V

+VCC_GT(U22): 31A(MAX)
+VCC_GT(U42): 28A(MAX)



Security Classification		Compal Secret Data		Title	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	MCP(11/14)PWR-VCCGT	
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Date:		Friday, July 28, 2017		Sheet	16 of 65

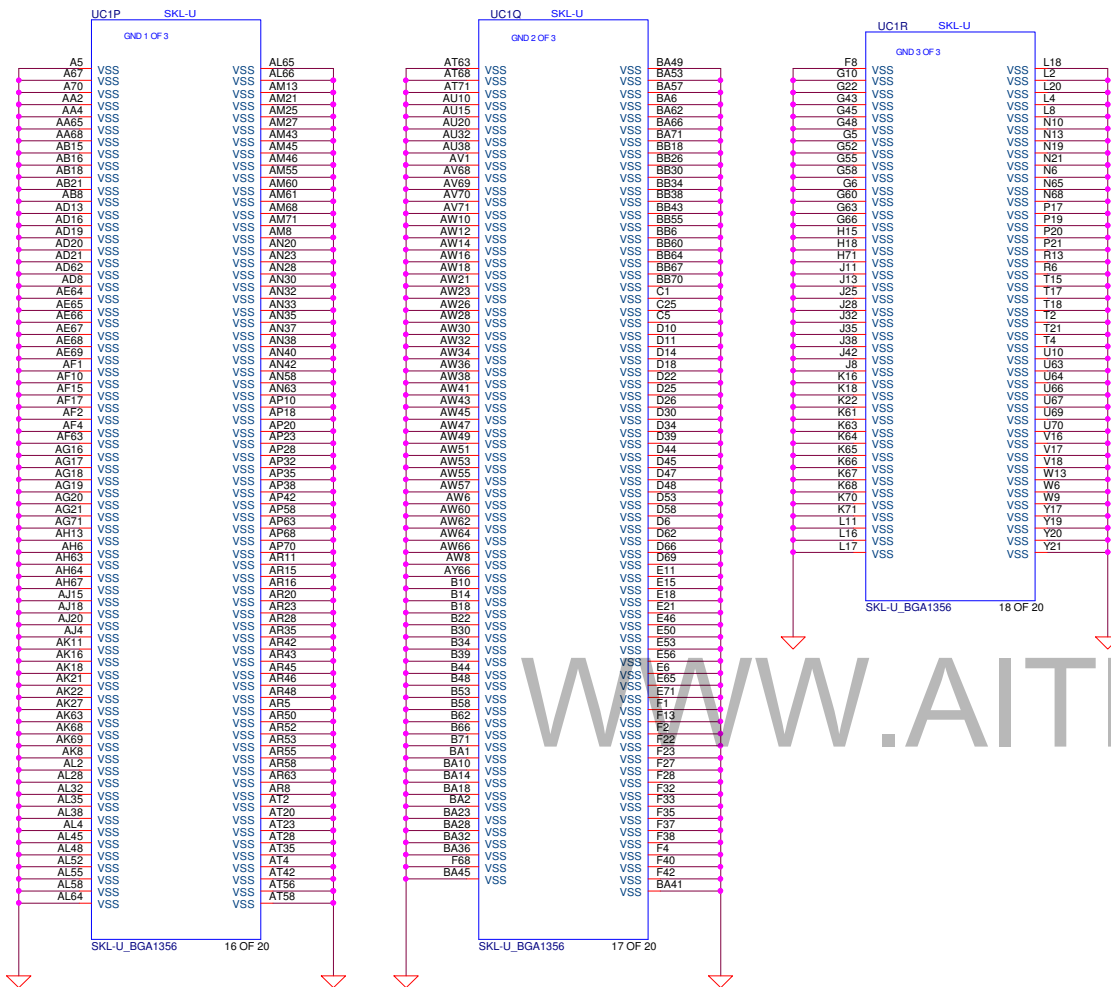
+1.0V_MPHYGT source

PCH PWR



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Main Func = CPU



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.

- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

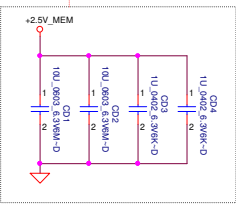
For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

Security Classification				Compal Secret Data				Title			
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Date:				Friday, July 28, 2017		Sheet		19		of 65	

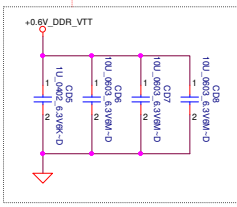
Main Func = DDR

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<7> DDR_A MA0_013
<7> DDR_A DQ50_07
<7> DDR_A DQ50_07

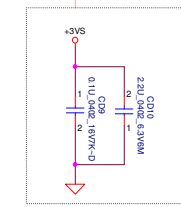
Layout Note:
Place near JDIMM1.257,259



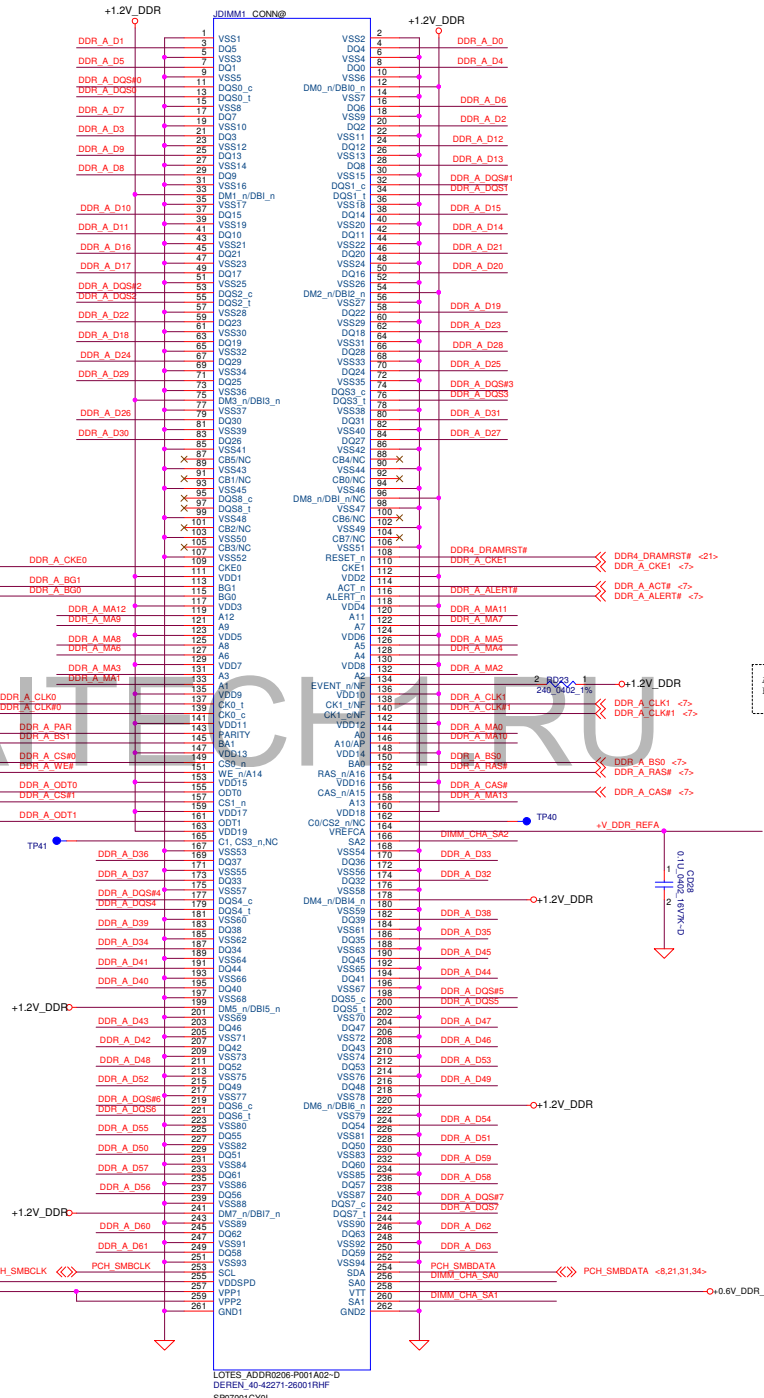
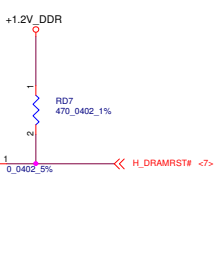
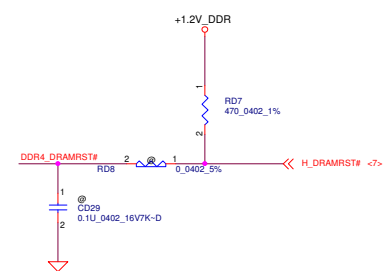
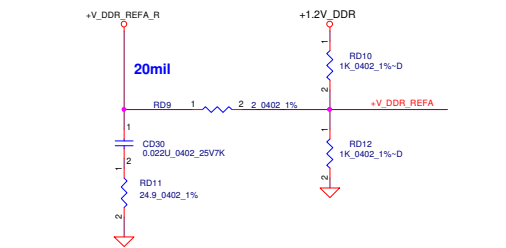
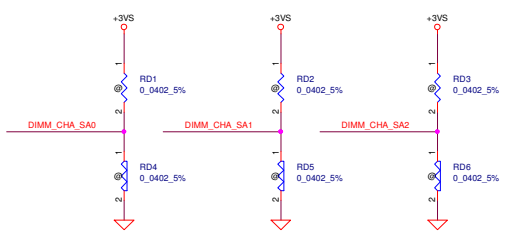
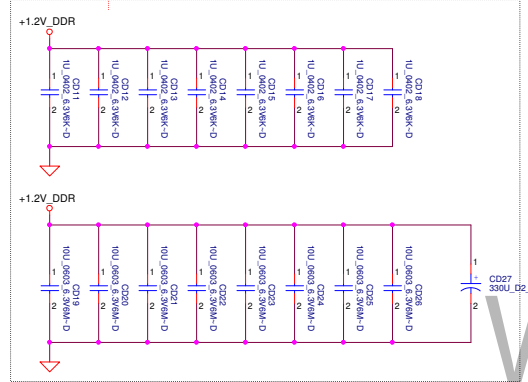
Layout Note:
Place near JDIMM1.258



Layout Note:
Place near JDIMM1.255



Layout Note:
Place near JDIMM1

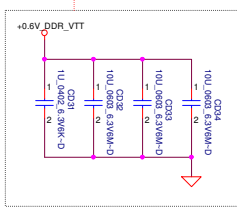


All VREF traces should
have 10 mil trace width

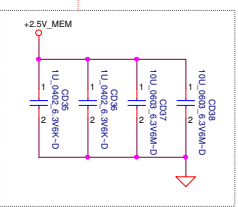
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Issued Date	2016/12/01	Deciphered Date	2017/12/01	Compal Electronics, Inc.	
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				LA-F111P	0.1
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Main Func = DDR

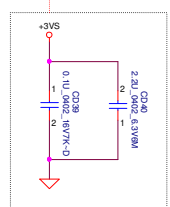
Layout Note:
Place near JDIMM2.258



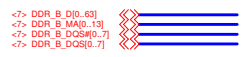
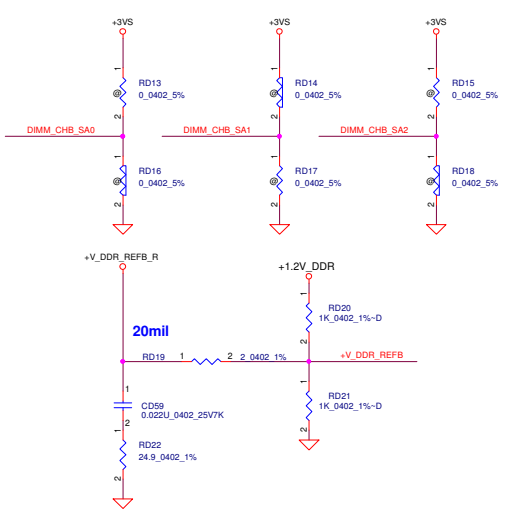
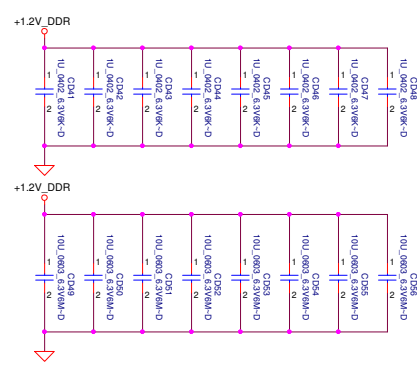
Layout Note:
Place near JDIMM2.257,259



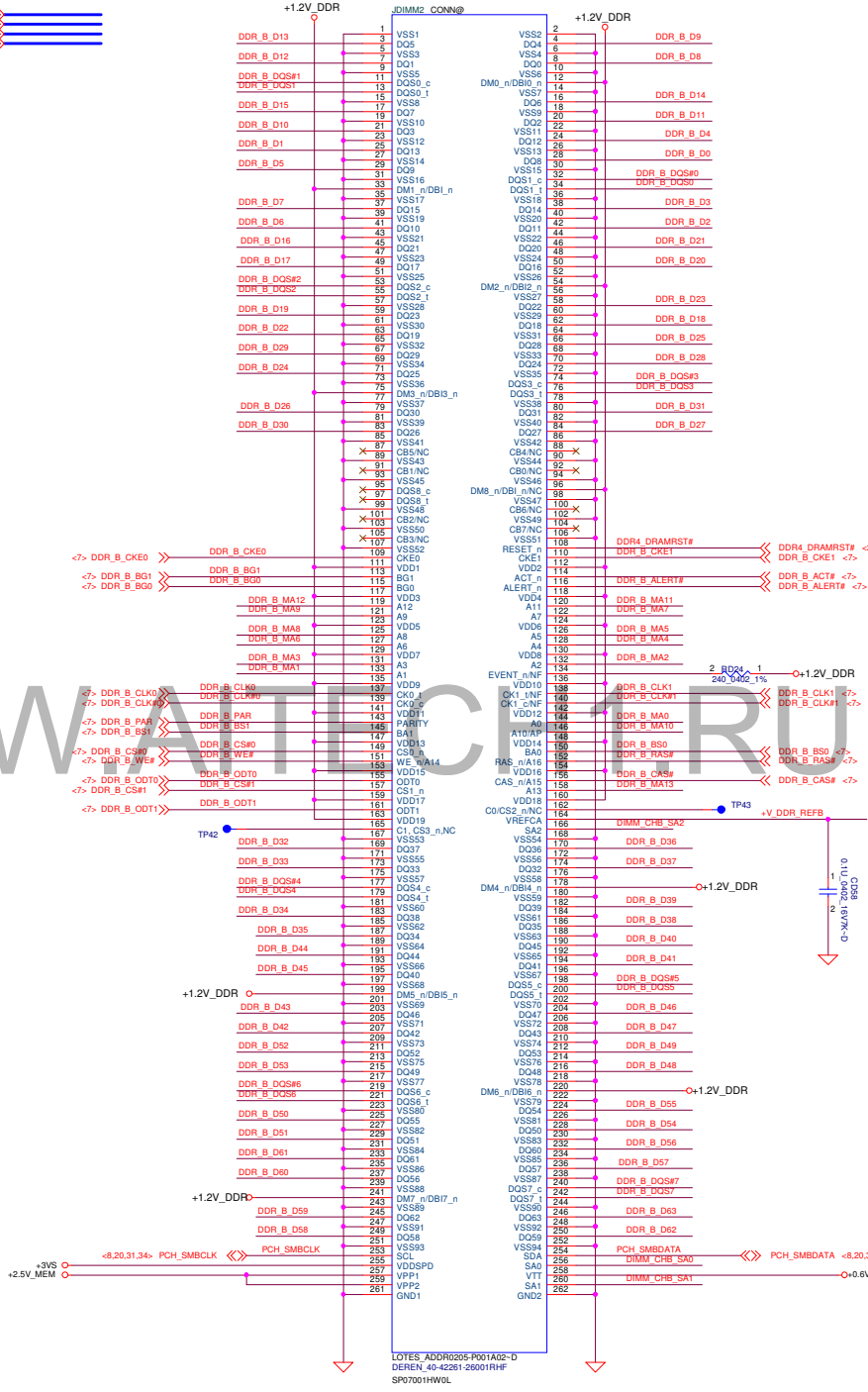
Layout Note:
Place near JDIMM2.255



Layout Note:
Place near JDIMM2



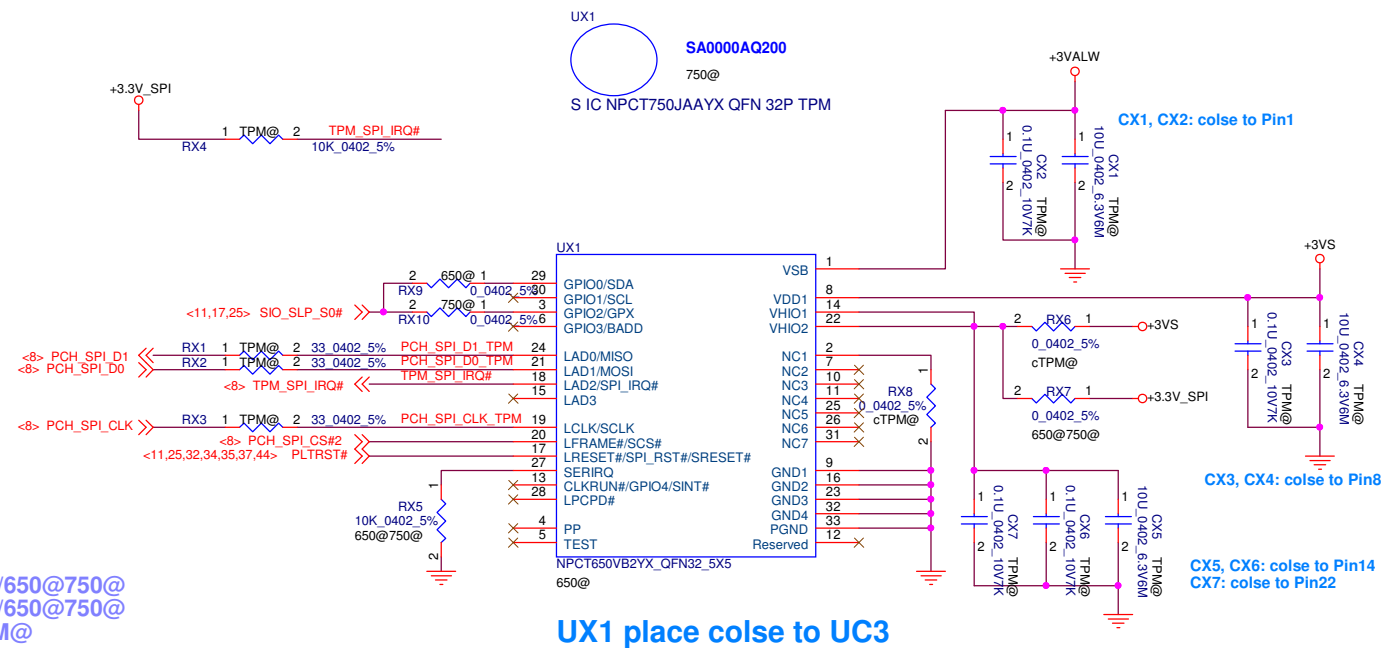
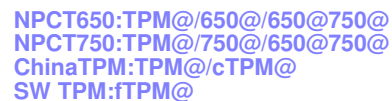
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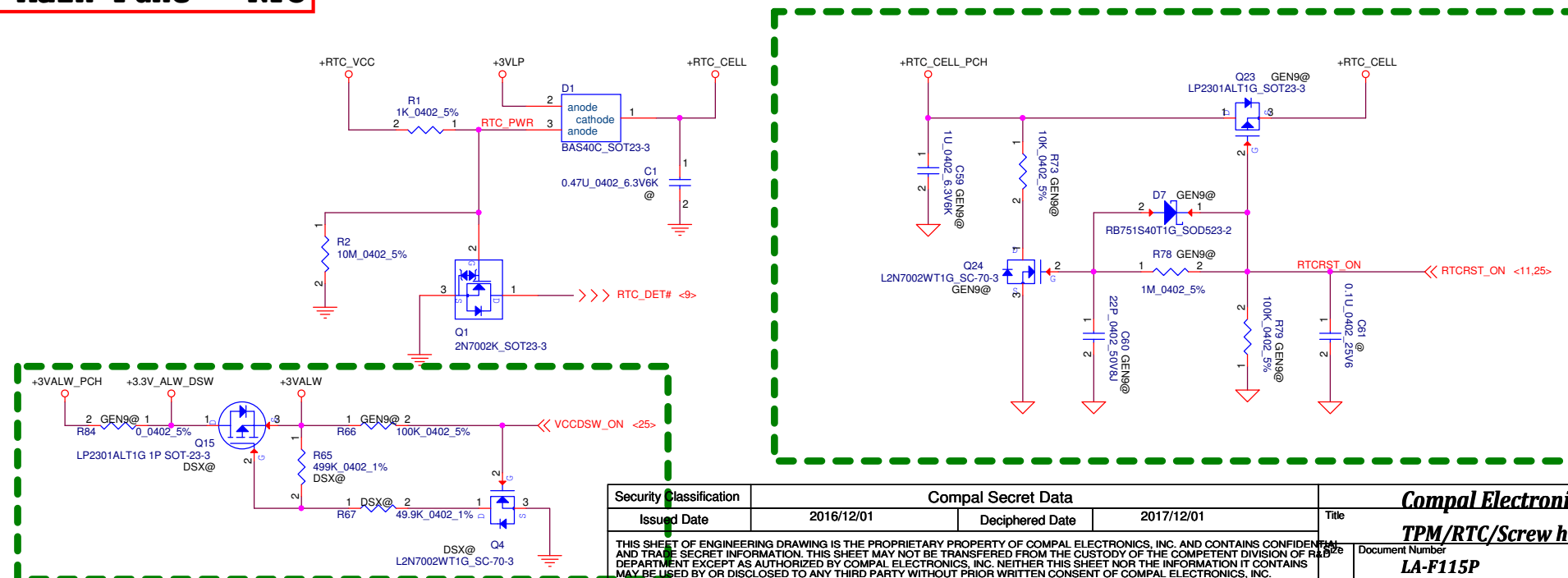
All VREF traces should
have 10 mil trace width

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Issued Date	2016/12/01	Deciphered Date	2017/12/01	DDR4 DIMMB STD	
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Screw hole/FD

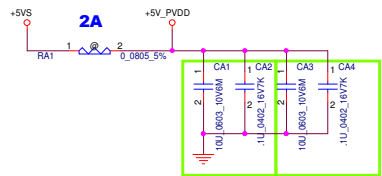


Main Func = RTC



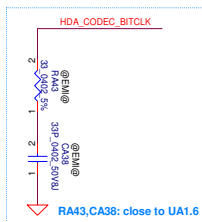
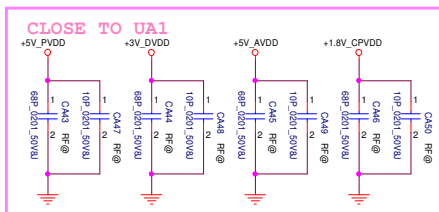
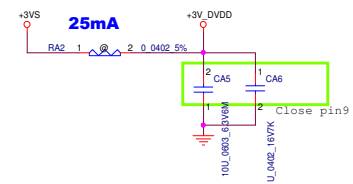
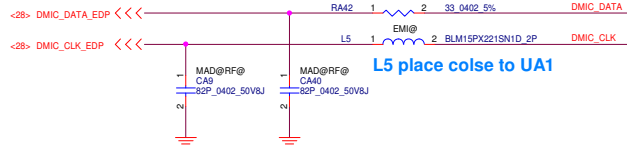
Security Classification		Compal Secret Data		Compal Electronics, Inc. TPM/RTC/Screw hole	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title	
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Date: Friday, July 28, 2017		Sheet 22 of 65			

Main Func = Audio

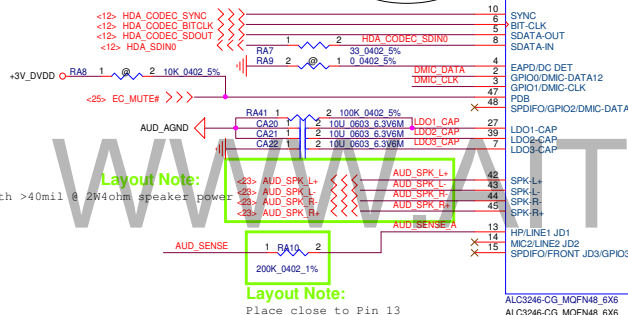


Layout Note:
Close pin41

Layout Note:
Close pin46

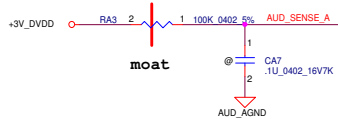


Speaker trace width >40mil @ 2W4ohm speaker power



Layout Note:

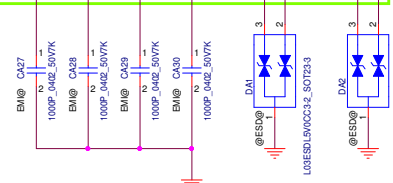
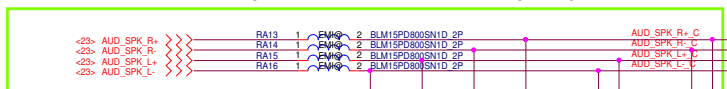
Layout Note:
Place close to Pin 13



Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

Speaker



ISPK1

ISPK2

G1

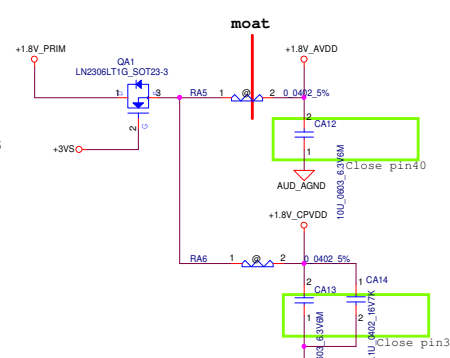
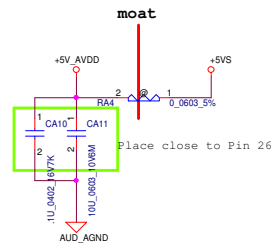
G2

ACES 50224-00401-001

CONN@

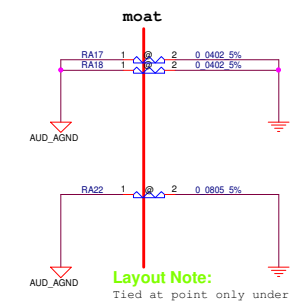
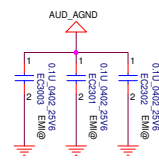
SP02000GC10

CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Layout Note:

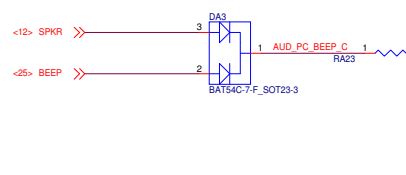
Width>40mil, to improve Headphone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.



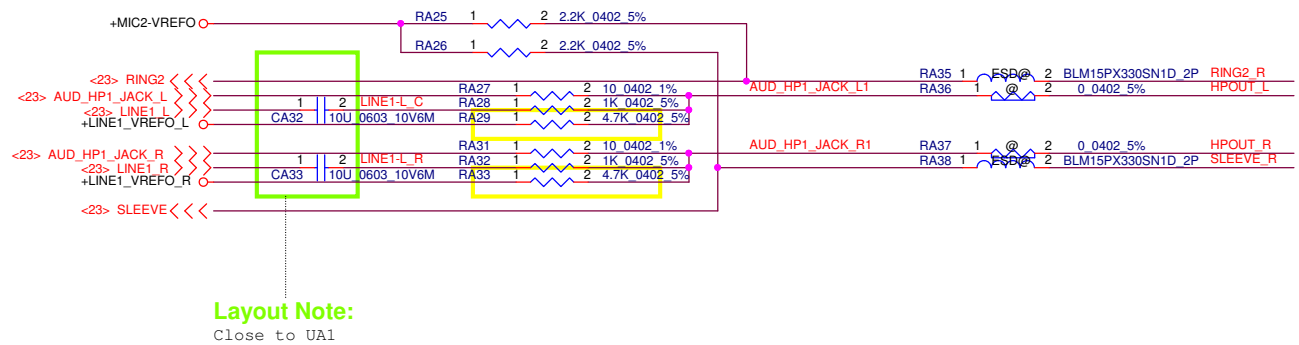
Layout Note:

Tied at point only under
Codec or near the Codec

Place on the moat between GND & GNDA.

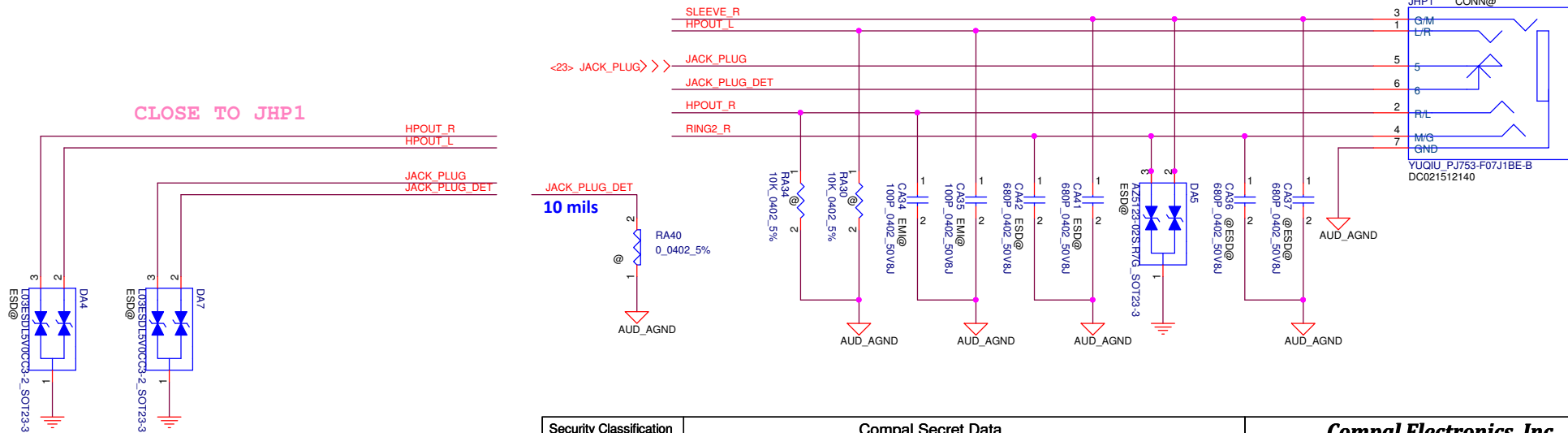


Main Func = Audio Jack



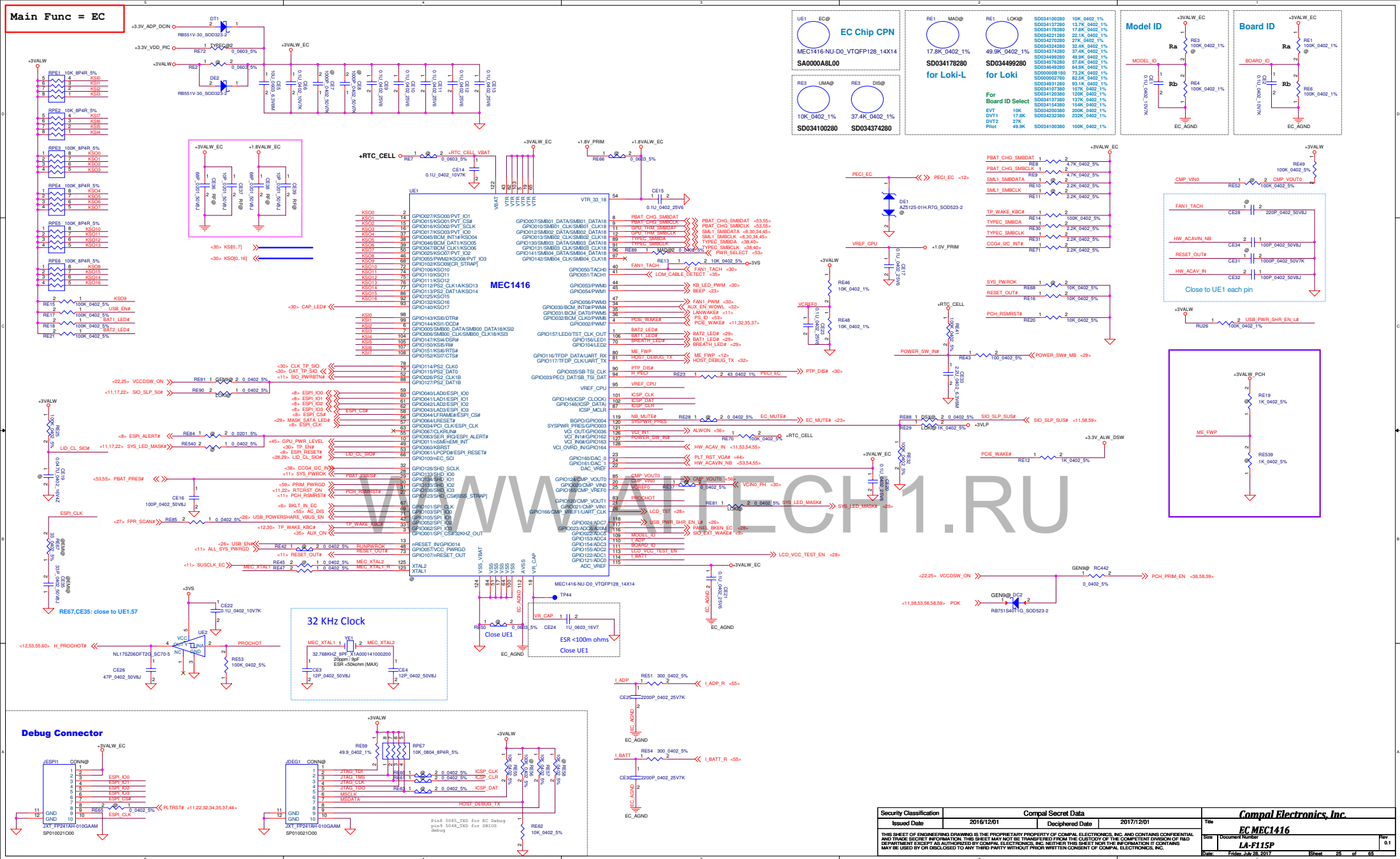
Universal Jack
(Global Headset Jack + mic phone in + line in support)

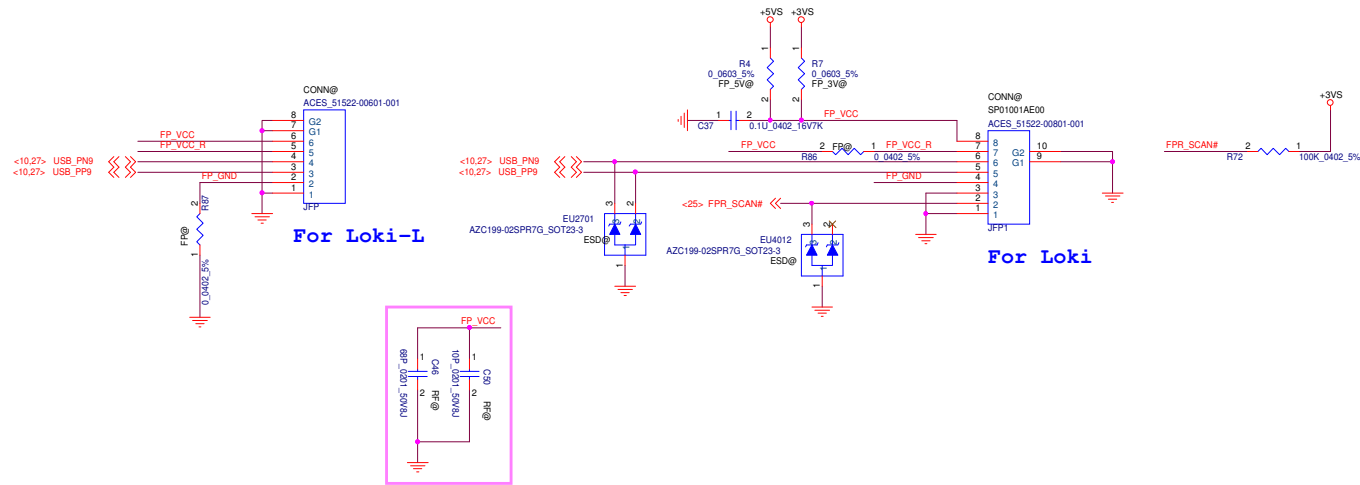
Main Func = Audio Jack



Universal Jack
(Global Headset Jack + mic phone in + line in support)

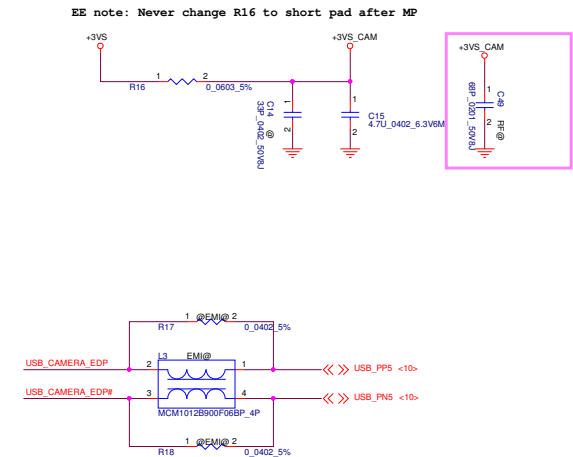
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2016/12/01		Deciphered Date		2017/12/01		Title			
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						Document Number				Rev	
						LA-F115P				0.1	
						Date: Friday, July 28, 2017		Sheet 24 of 65			



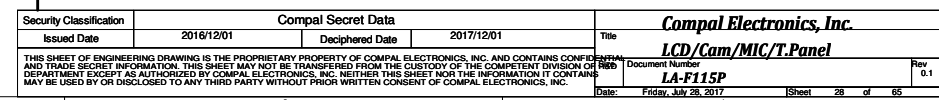
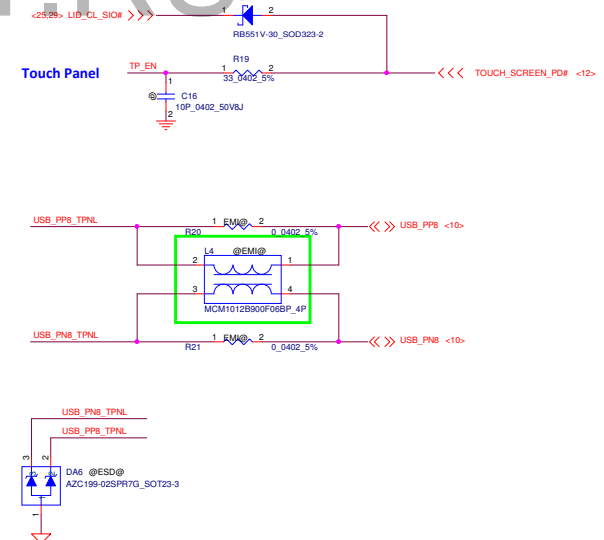


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Main Func = CAM

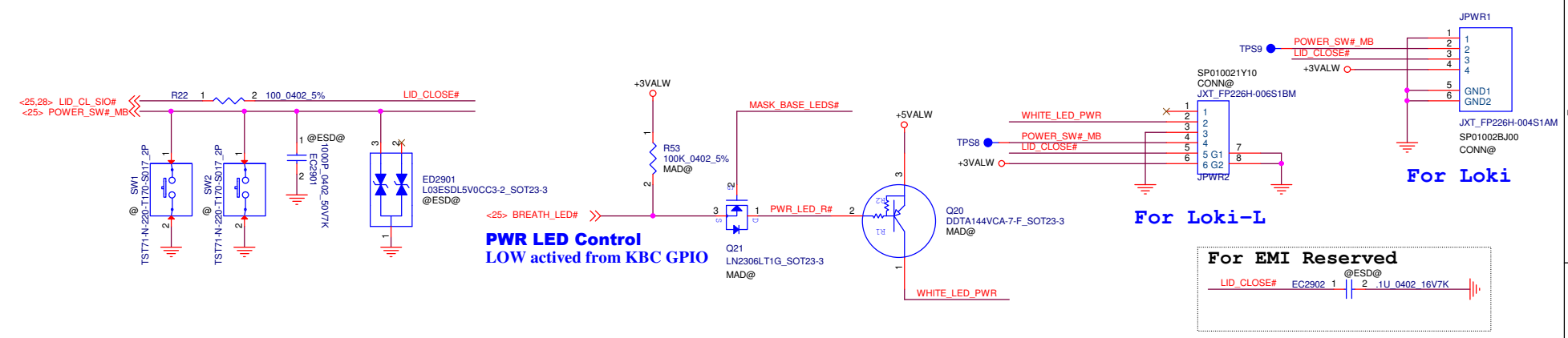


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Main Func = Power BTN Main Func = PWR LED

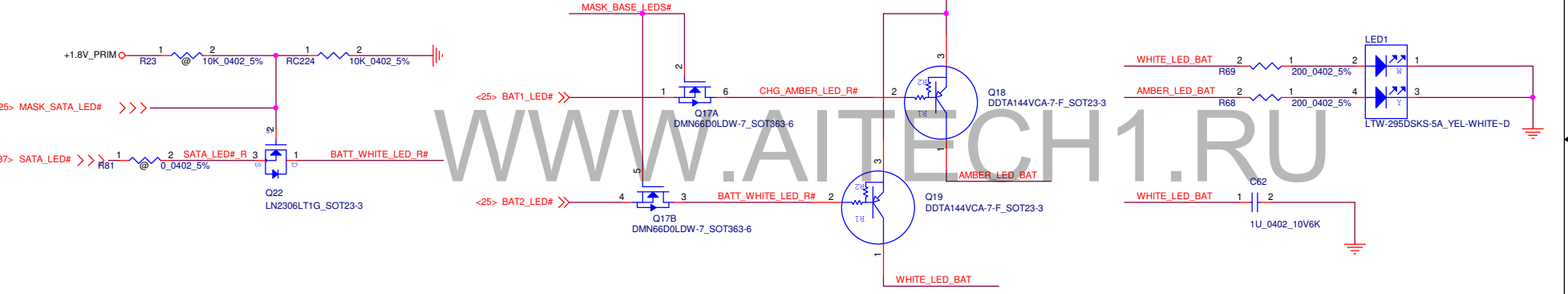
Low actived from KBC GPIO



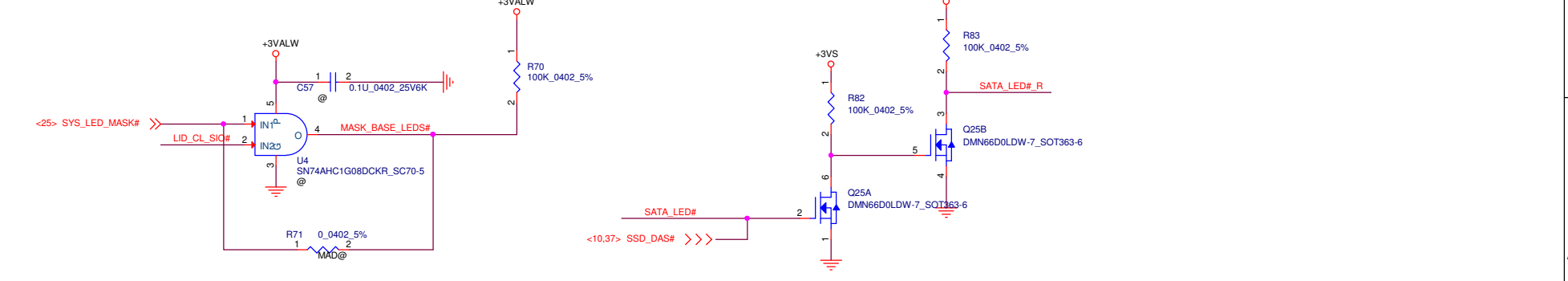
Main Func = Battery LED

BJT
R1: 47 K
R2: 10 K

Low actived from KBC GPIO

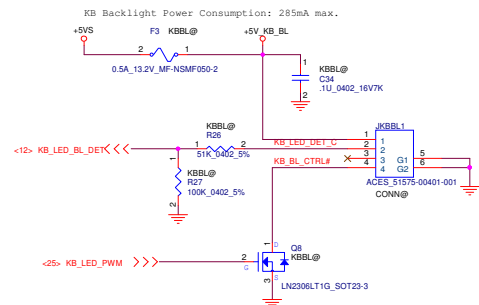
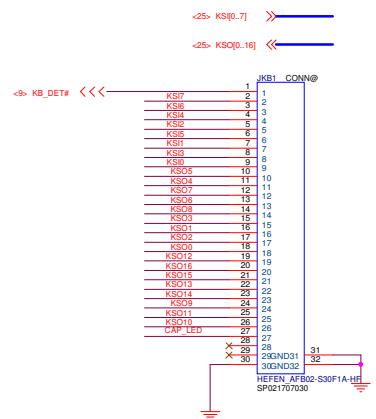


Main Func = Unobtrusive Mode

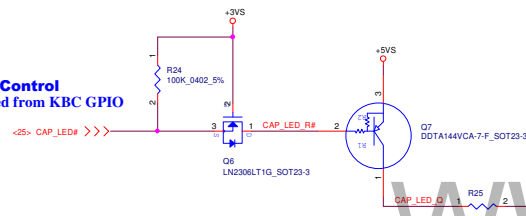


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Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title	LED Board/Power Button	
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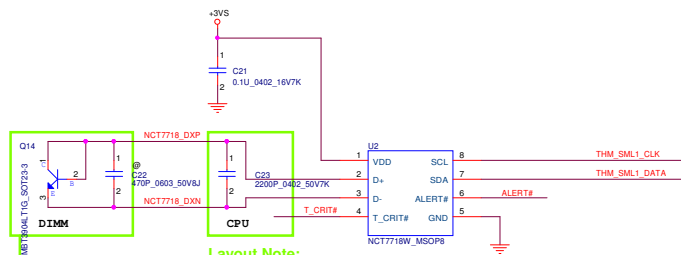
Main Func = KE



For EMI Reserved



Main Func = Thermal



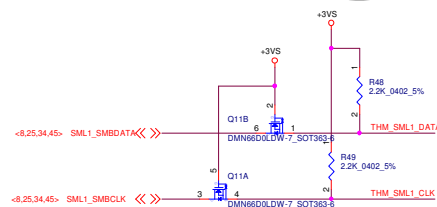
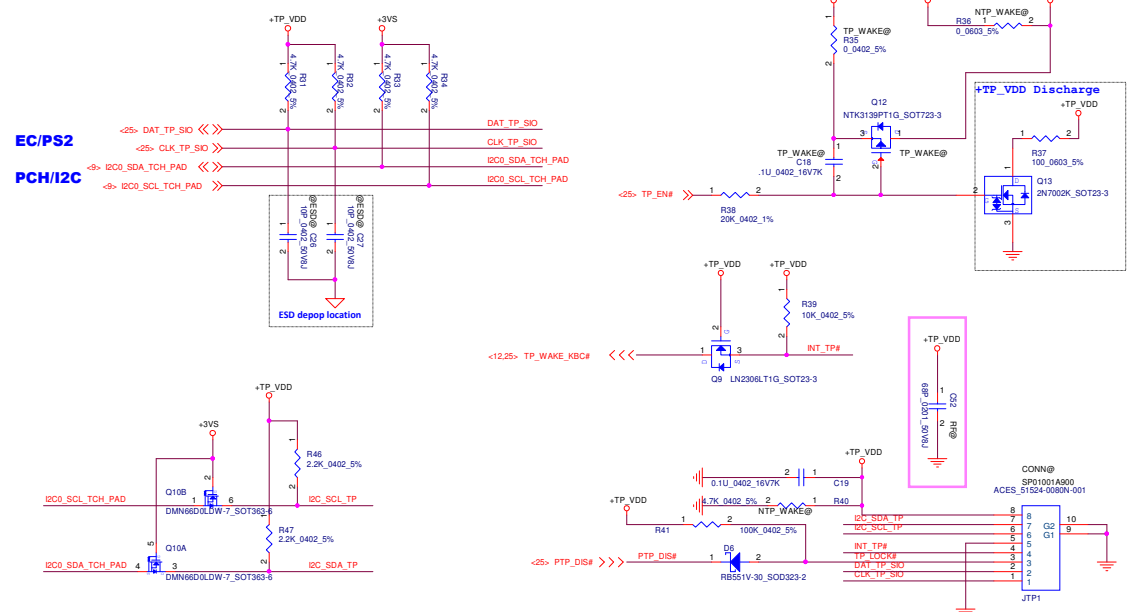
DXN and DXP routing width and spacing is 10 mil / 10 mil.

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

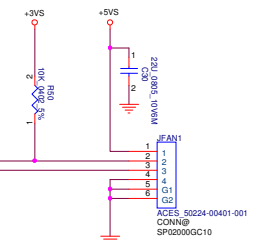
3
Main Func = TPAD

EC/PS2

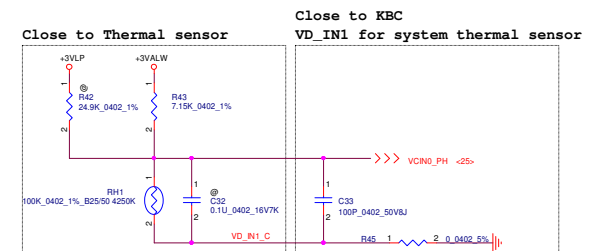
PCH/I2C



"FAN1_FB" PU 10k on EC side



Main Func = OTP



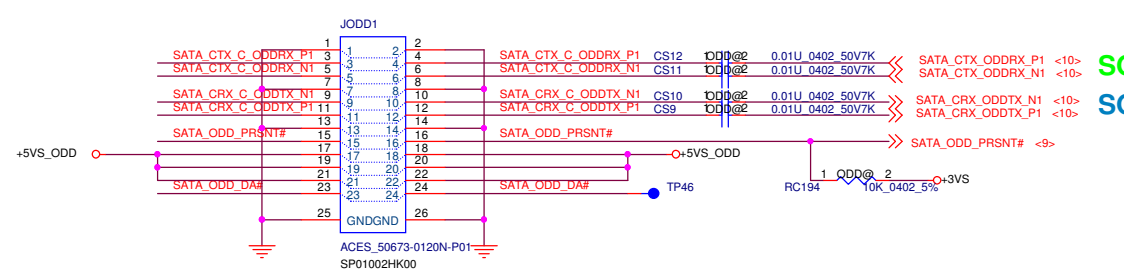
Security Classification		Compal Secret Data		Title	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Keyboard/Touch Pad/Thermal/FAN	
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Date:		Expiry:		Date:	

Main Func = HDD&FFS



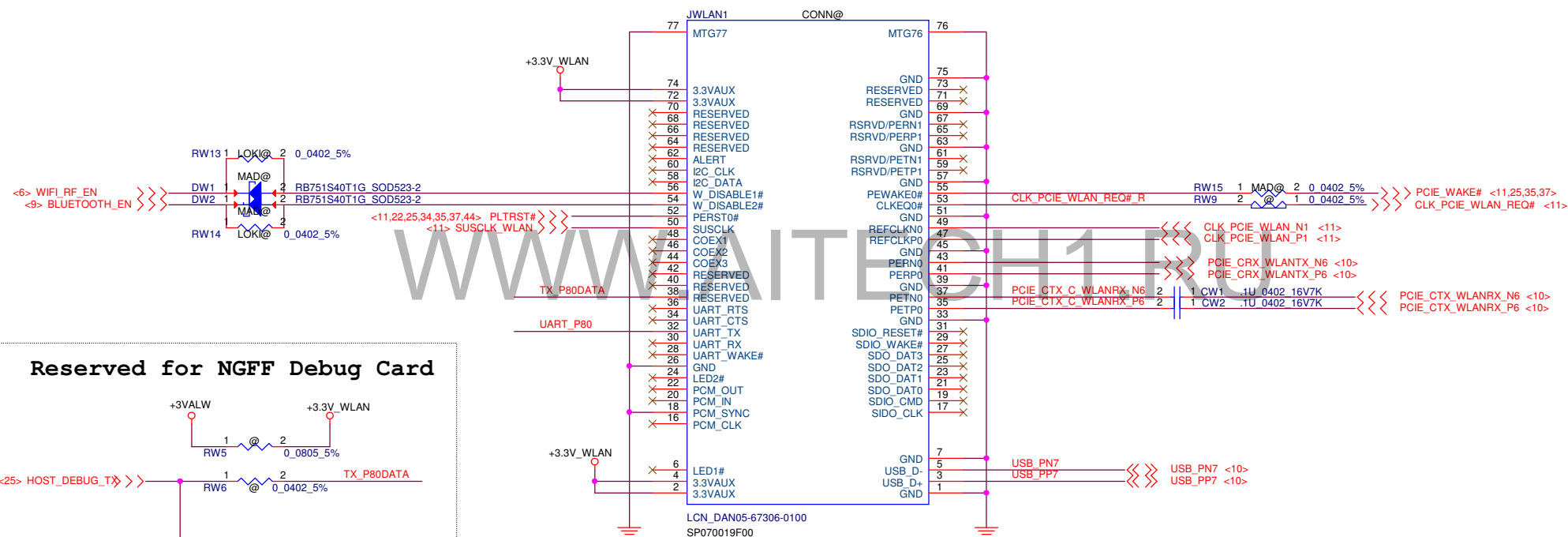
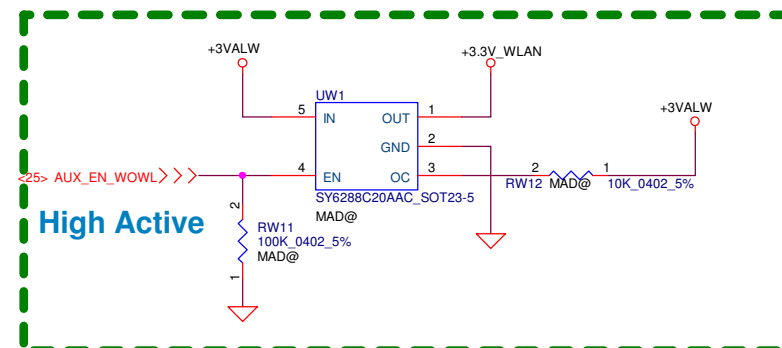
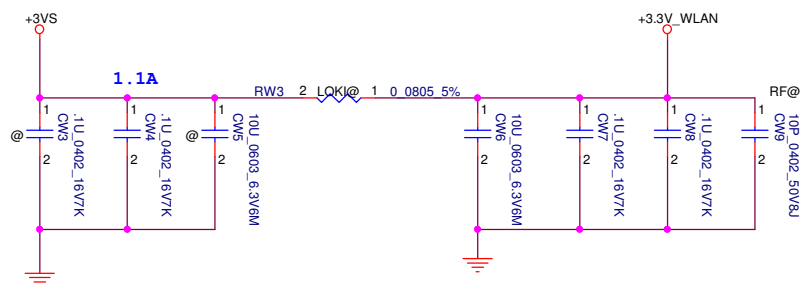
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSENT	P1	8
5V	P2	9 10 11
5V	P3	
Attention	P4	12
GND	P5	
GND	P6	

Main Func = ODD

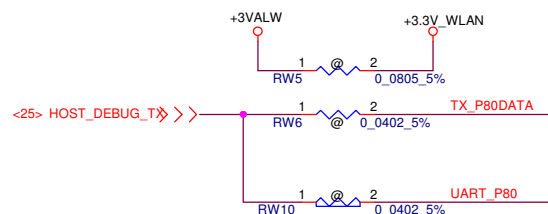


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Main Func = WLAN

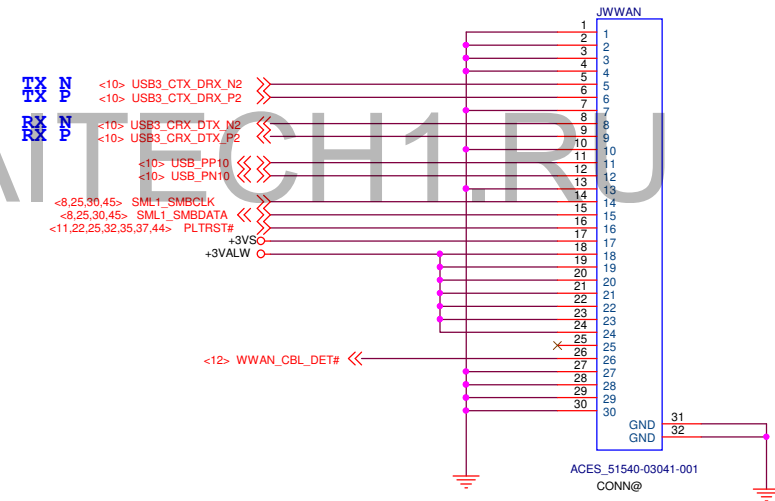
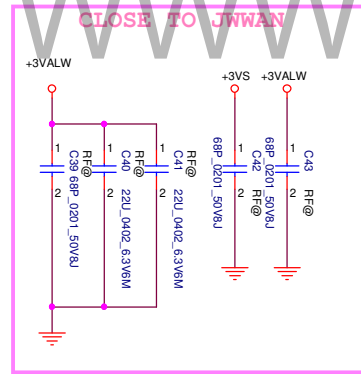
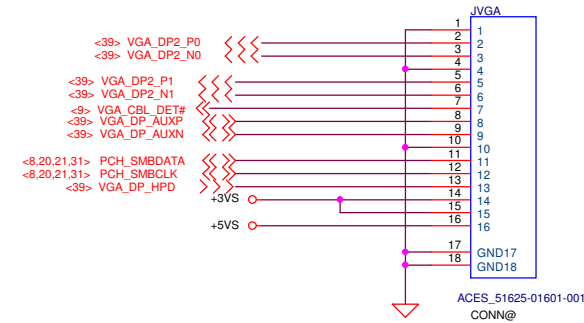


Reserved for NGFF Debug Card



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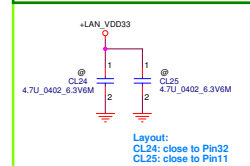
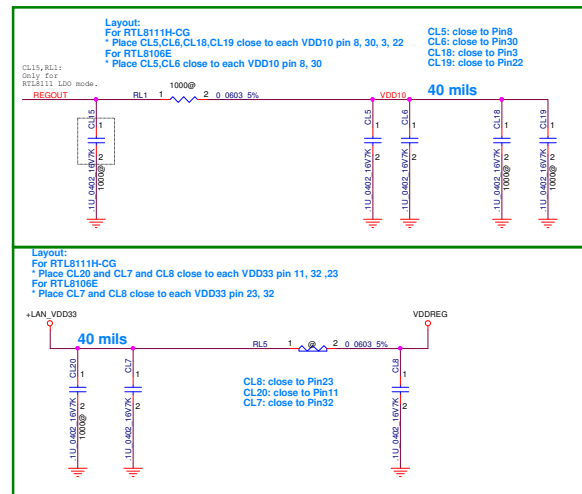
Main Func = WWAN/B & VGA/B



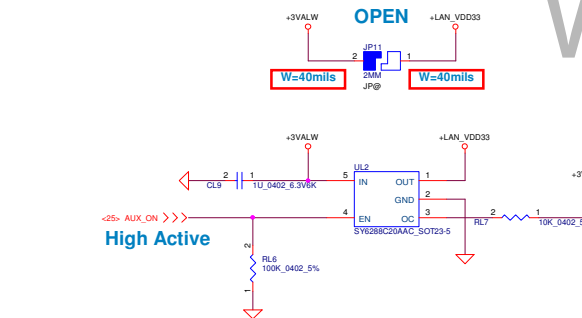
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2016/12/01				Deciphered Date			
2017/12/01				Title				IO DB(WWAN/VGA)			
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65				Rev				0.1			

RTL8111G-CGT (71.08111.U03/LDO Mode): 10/100/1000M < 252 mW.
RTL8106E-CG (071.08106.0003): 10/100M < 70mW.

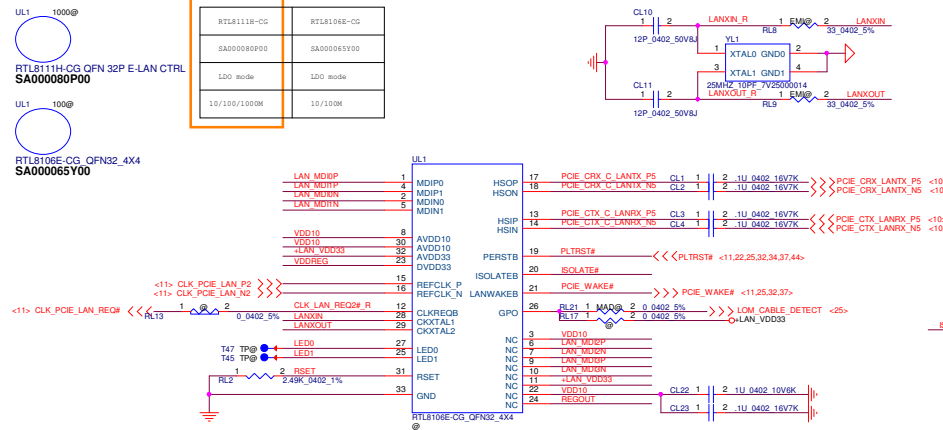
Main Func = LAN



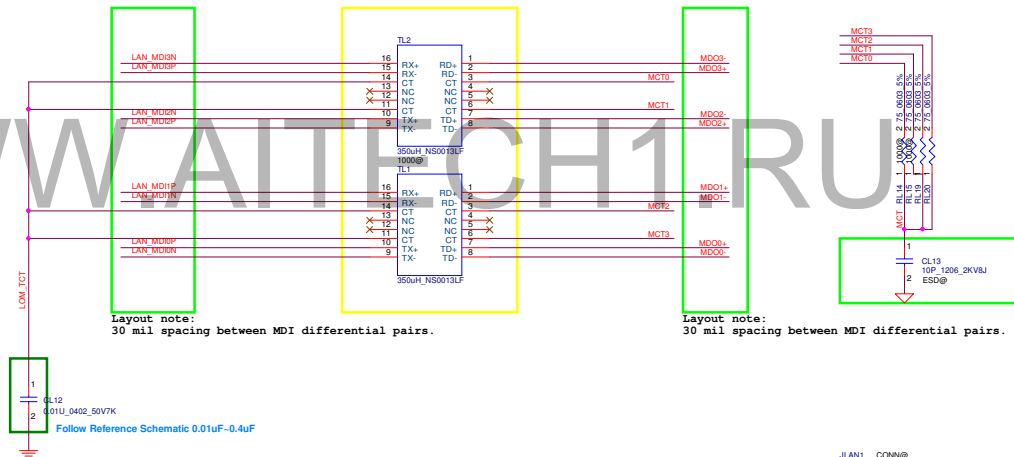
+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



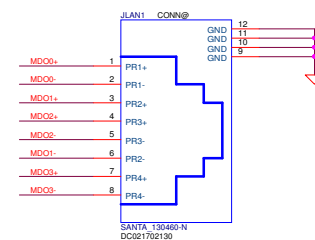
LAN Chip (10/100/1000M & 10/100M co-layout)



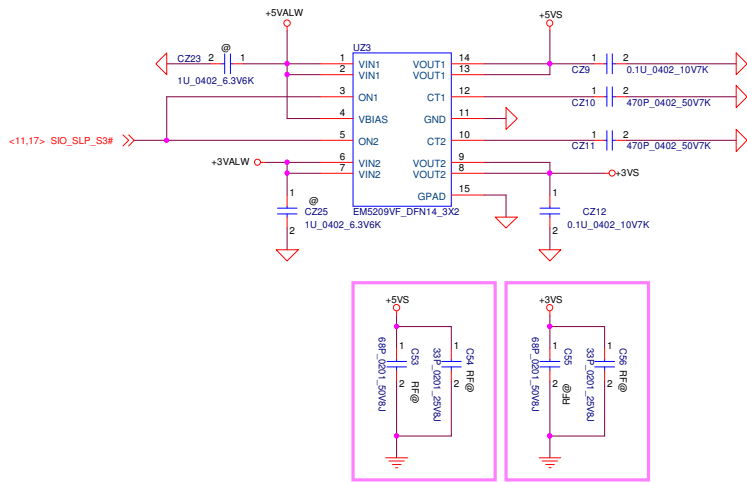
LAN TransFormer (10/100/1000M & 10/100M co-layout)



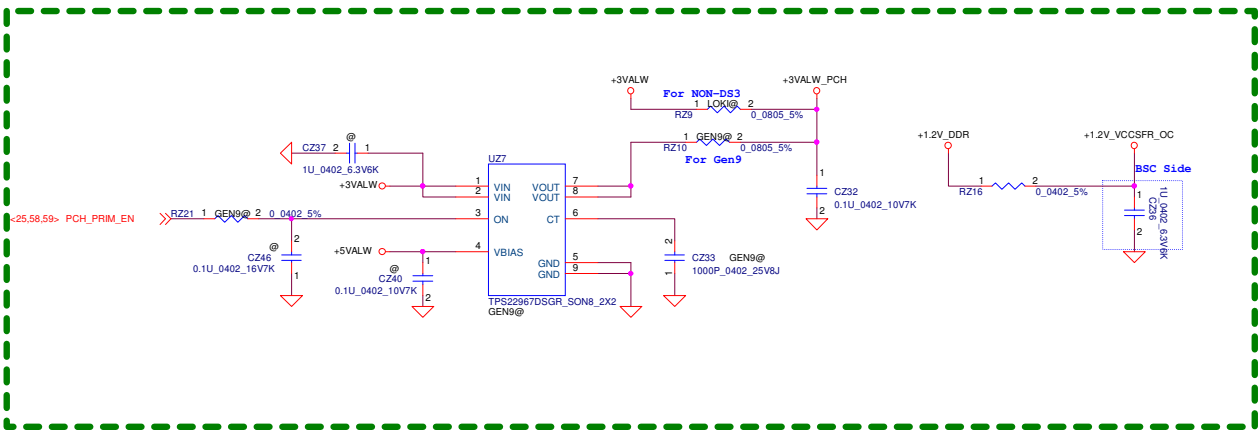
	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O



+5VS/+3VS for System



+3VALW_PCH for System
+1.2V_DDR TO +1.2V_VCCSFR_OC

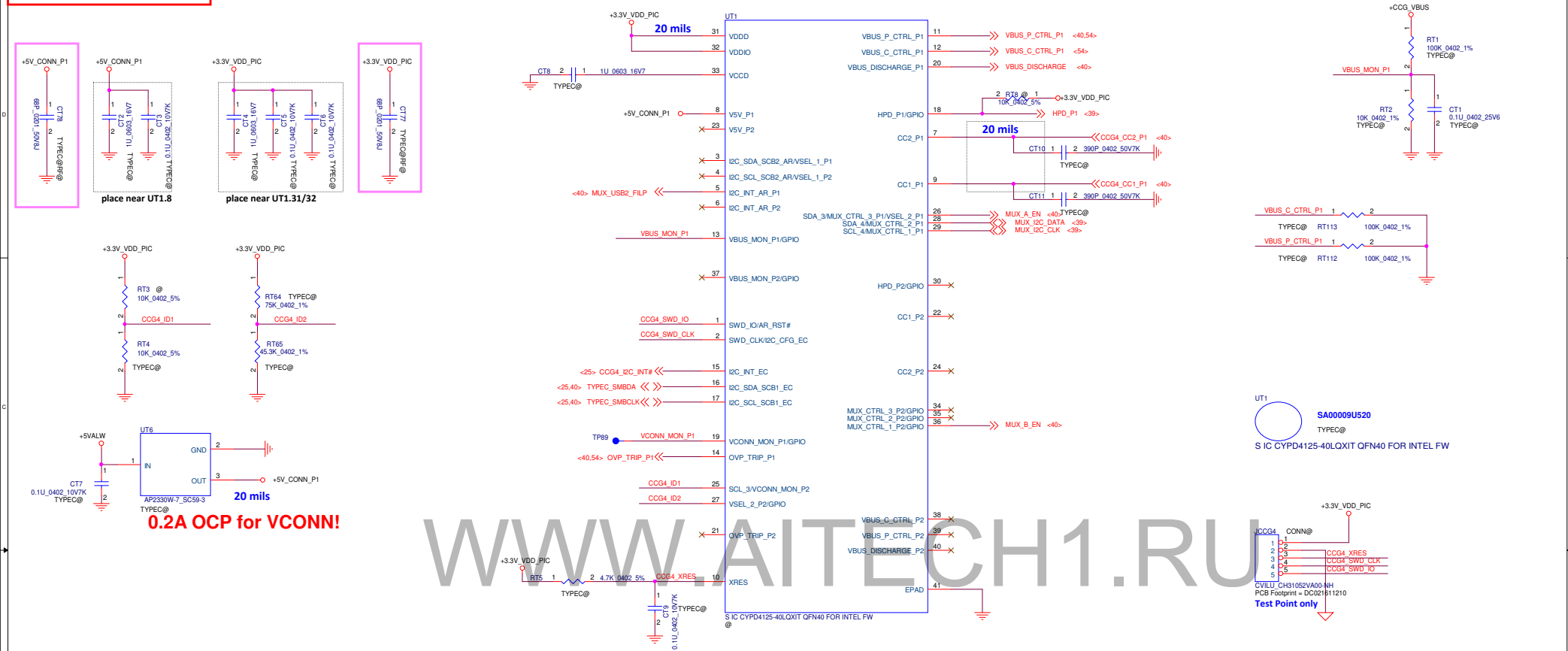


NON-DSX (LOKI)
DSX (LOKI-L)

WWW.AITECH1.RU

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				Date:	Friday, July 28, 2017	Sheet 36 of 65

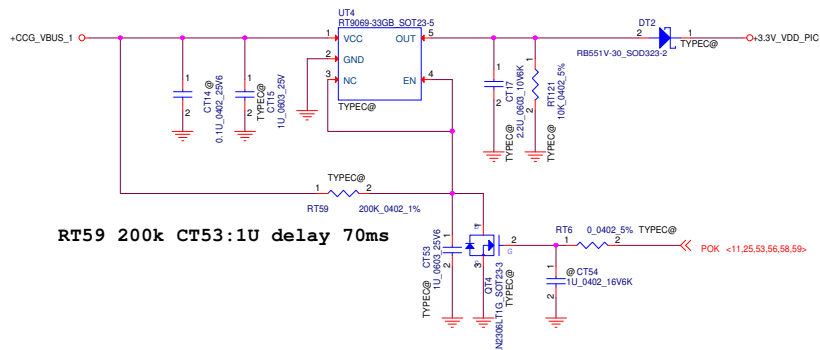
Main Func = CCG4

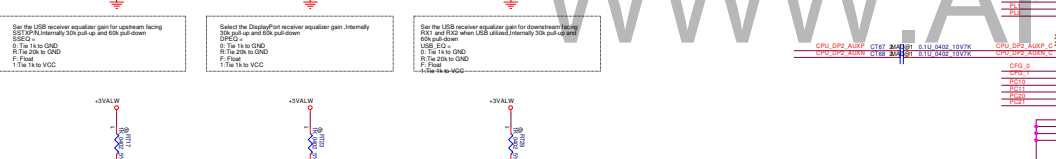
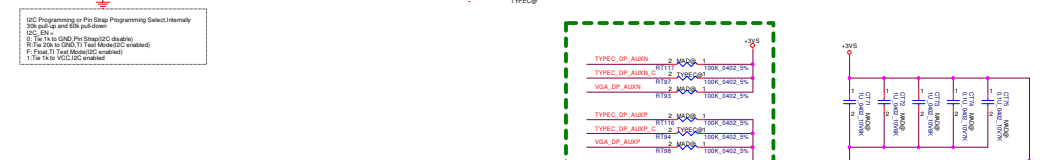


Voltages for various platform on "CCG4_ID_1" pin and "CCG4_ID_2" pin

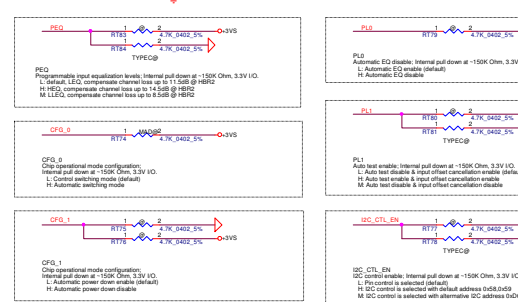
#	Platform	Voltage on CCGA_ID_1	Voltage on CCGA_ID_2
1	Single Port - Intel - DDM support - Armani 13" & 14"	L0	L7
2	Single Port - Intel - DDM support - <u>Kyloren</u>	L0	L6
3	Single Port - Intel - DDM support - <u>Miyake</u>	L0	L5
4	Single Port - Intel - DDM support - Loki 13"	L0	L4
5	Single Port - Intel - DDM support - Loki 15" & 17" (Motherboard is same)	L0	L3
6	Single Port - Intel - DDM support - <u>StarLord</u> KBL - R	L0	L2
7	Single Port - AMD - DDM not supported - Loki 15" & 17" (Motherboard is same)	L4	L0

Voltage level	Voltage value
L0	0V
L1	3.3V
L2	3.3V/2
L3	3.3V/3
L4	3.3V/4
L5	3.3V/5
L6	3.3V/6
L7	3.3V/7

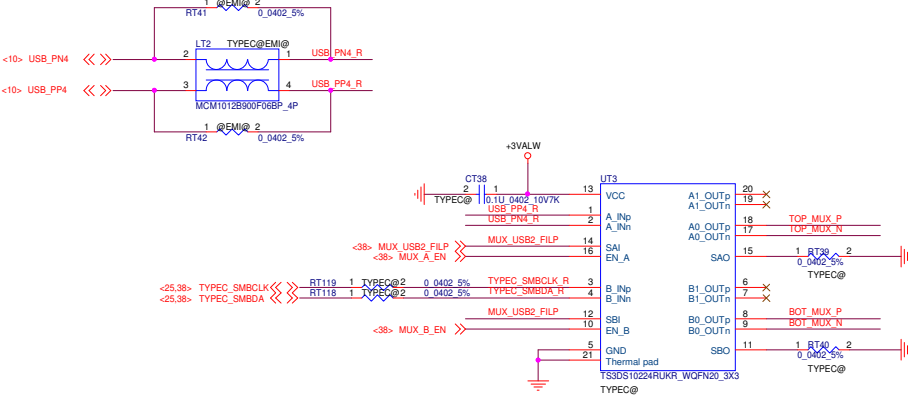




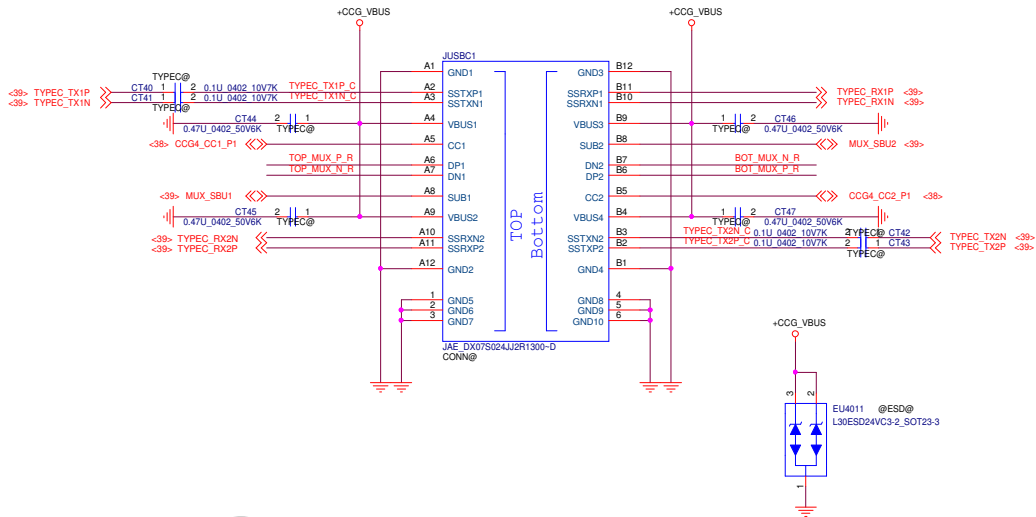
		HPS P1	LOWP2P3	CPU DP2 HPS				
		RT101	RT101	RT101	RT101	RT101	RT101	RT101
-> CPU DP2 P0	CPU DP2 P0	RT101	LOWP2P3	0.0001 S	DP P0	RT101	LOWP2P3	0.0001 S
-> CPU DP2 N0	CPU DP2 N0	RT101	LOWP2P3	0.0001 S	DP N0	RT101	LOWP2P3	0.0001 S
-> CPU DP2 P1	CPU DP2 P1	RT101	LOWP2P3	0.0001 S	DP P1	RT101	LOWP2P3	0.0001 S
-> CPU DP2 N1	CPU DP2 N1	RT101	LOWP2P3	0.0001 S	DP N1	RT101	LOWP2P3	0.0001 S
-> CPU DP2 P2	CPU DP2 P2	RT101	LOWP2P3	0.0001 S	DP P2	RT101	LOWP2P3	0.0001 S
-> CPU DP2 N2	CPU DP2 N2	RT101	LOWP2P3	0.0001 S	DP N2	RT101	LOWP2P3	0.0001 S
-> CPU DP2 P3	CPU DP2 P3	RT101	LOWP2P3	0.0001 S	DP P3	RT101	LOWP2P3	0.0001 S
-> CPU DP2 N3	CPU DP2 N3	RT101	LOWP2P3	0.0001 S	DP N3	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL0	CPU DP2 AL0	RT101	LOWP2P3	0.0001 S	DP AL0	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL1	CPU DP2 AL1	RT101	LOWP2P3	0.0001 S	DP AL1	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL2	CPU DP2 AL2	RT101	LOWP2P3	0.0001 S	DP AL2	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL3	CPU DP2 AL3	RT101	LOWP2P3	0.0001 S	DP AL3	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL4	CPU DP2 AL4	RT101	LOWP2P3	0.0001 S	DP AL4	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL5	CPU DP2 AL5	RT101	LOWP2P3	0.0001 S	DP AL5	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL6	CPU DP2 AL6	RT101	LOWP2P3	0.0001 S	DP AL6	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL7	CPU DP2 AL7	RT101	LOWP2P3	0.0001 S	DP AL7	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL8	CPU DP2 AL8	RT101	LOWP2P3	0.0001 S	DP AL8	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL9	CPU DP2 AL9	RT101	LOWP2P3	0.0001 S	DP AL9	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL10	CPU DP2 AL10	RT101	LOWP2P3	0.0001 S	DP AL10	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL11	CPU DP2 AL11	RT101	LOWP2P3	0.0001 S	DP AL11	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL12	CPU DP2 AL12	RT101	LOWP2P3	0.0001 S	DP AL12	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL13	CPU DP2 AL13	RT101	LOWP2P3	0.0001 S	DP AL13	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL14	CPU DP2 AL14	RT101	LOWP2P3	0.0001 S	DP AL14	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL15	CPU DP2 AL15	RT101	LOWP2P3	0.0001 S	DP AL15	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL16	CPU DP2 AL16	RT101	LOWP2P3	0.0001 S	DP AL16	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL17	CPU DP2 AL17	RT101	LOWP2P3	0.0001 S	DP AL17	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL18	CPU DP2 AL18	RT101	LOWP2P3	0.0001 S	DP AL18	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL19	CPU DP2 AL19	RT101	LOWP2P3	0.0001 S	DP AL19	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL20	CPU DP2 AL20	RT101	LOWP2P3	0.0001 S	DP AL20	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL21	CPU DP2 AL21	RT101	LOWP2P3	0.0001 S	DP AL21	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL22	CPU DP2 AL22	RT101	LOWP2P3	0.0001 S	DP AL22	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL23	CPU DP2 AL23	RT101	LOWP2P3	0.0001 S	DP AL23	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL24	CPU DP2 AL24	RT101	LOWP2P3	0.0001 S	DP AL24	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL25	CPU DP2 AL25	RT101	LOWP2P3	0.0001 S	DP AL25	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL26	CPU DP2 AL26	RT101	LOWP2P3	0.0001 S	DP AL26	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL27	CPU DP2 AL27	RT101	LOWP2P3	0.0001 S	DP AL27	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL28	CPU DP2 AL28	RT101	LOWP2P3	0.0001 S	DP AL28	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL29	CPU DP2 AL29	RT101	LOWP2P3	0.0001 S	DP AL29	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL30	CPU DP2 AL30	RT101	LOWP2P3	0.0001 S	DP AL30	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL31	CPU DP2 AL31	RT101	LOWP2P3	0.0001 S	DP AL31	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL32	CPU DP2 AL32	RT101	LOWP2P3	0.0001 S	DP AL32	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL33	CPU DP2 AL33	RT101	LOWP2P3	0.0001 S	DP AL33	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL34	CPU DP2 AL34	RT101	LOWP2P3	0.0001 S	DP AL34	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL35	CPU DP2 AL35	RT101	LOWP2P3	0.0001 S	DP AL35	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL36	CPU DP2 AL36	RT101	LOWP2P3	0.0001 S	DP AL36	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL37	CPU DP2 AL37	RT101	LOWP2P3	0.0001 S	DP AL37	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL38	CPU DP2 AL38	RT101	LOWP2P3	0.0001 S	DP AL38	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL39	CPU DP2 AL39	RT101	LOWP2P3	0.0001 S	DP AL39	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL40	CPU DP2 AL40	RT101	LOWP2P3	0.0001 S	DP AL40	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL41	CPU DP2 AL41	RT101	LOWP2P3	0.0001 S	DP AL41	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL42	CPU DP2 AL42	RT101	LOWP2P3	0.0001 S	DP AL42	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL43	CPU DP2 AL43	RT101	LOWP2P3	0.0001 S	DP AL43	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL44	CPU DP2 AL44	RT101	LOWP2P3	0.0001 S	DP AL44	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL45	CPU DP2 AL45	RT101	LOWP2P3	0.0001 S	DP AL45	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL46	CPU DP2 AL46	RT101	LOWP2P3	0.0001 S	DP AL46	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL47	CPU DP2 AL47	RT101	LOWP2P3	0.0001 S	DP AL47	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL48	CPU DP2 AL48	RT101	LOWP2P3	0.0001 S	DP AL48	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL49	CPU DP2 AL49	RT101	LOWP2P3	0.0001 S	DP AL49	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL50	CPU DP2 AL50	RT101	LOWP2P3	0.0001 S	DP AL50	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL51	CPU DP2 AL51	RT101	LOWP2P3	0.0001 S	DP AL51	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL52	CPU DP2 AL52	RT101	LOWP2P3	0.0001 S	DP AL52	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL53	CPU DP2 AL53	RT101	LOWP2P3	0.0001 S	DP AL53	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL54	CPU DP2 AL54	RT101	LOWP2P3	0.0001 S	DP AL54	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL55	CPU DP2 AL55	RT101	LOWP2P3	0.0001 S	DP AL55	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL56	CPU DP2 AL56	RT101	LOWP2P3	0.0001 S	DP AL56	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL57	CPU DP2 AL57	RT101	LOWP2P3	0.0001 S	DP AL57	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL58	CPU DP2 AL58	RT101	LOWP2P3	0.0001 S	DP AL58	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL59	CPU DP2 AL59	RT101	LOWP2P3	0.0001 S	DP AL59	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL60	CPU DP2 AL60	RT101	LOWP2P3	0.0001 S	DP AL60	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL61	CPU DP2 AL61	RT101	LOWP2P3	0.0001 S	DP AL61	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL62	CPU DP2 AL62	RT101	LOWP2P3	0.0001 S	DP AL62	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL63	CPU DP2 AL63	RT101	LOWP2P3	0.0001 S	DP AL63	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL64	CPU DP2 AL64	RT101	LOWP2P3	0.0001 S	DP AL64	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL65	CPU DP2 AL65	RT101	LOWP2P3	0.0001 S	DP AL65	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL66	CPU DP2 AL66	RT101	LOWP2P3	0.0001 S	DP AL66	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL67	CPU DP2 AL67	RT101	LOWP2P3	0.0001 S	DP AL67	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL68	CPU DP2 AL68	RT101	LOWP2P3	0.0001 S	DP AL68	RT101	LOWP2P3	0.0001 S
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-> CPU DP2 AL84	CPU DP2 AL84	RT101	LOWP2P3	0.0001 S	DP AL84	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL85	CPU DP2 AL85	RT101	LOWP2P3	0.0001 S	DP AL85	RT101	LOWP2P3	0.0001 S
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-> CPU DP2 AL89	CPU DP2 AL89	RT101	LOWP2P3	0.0001 S	DP AL89	RT101	LOWP2P3	0.0001 S
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-> CPU DP2 AL93	CPU DP2 AL93	RT101	LOWP2P3	0.0001 S	DP AL93	RT101	LOWP2P3	0.0001 S
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-> CPU DP2 AL99	CPU DP2 AL99	RT101	LOWP2P3	0.0001 S	DP AL99	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL100	CPU DP2 AL100	RT101	LOWP2P3	0.0001 S	DP AL100	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL101	CPU DP2 AL101	RT101	LOWP2P3	0.0001 S	DP AL101	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL102	CPU DP2 AL102	RT101	LOWP2P3	0.0001 S	DP AL102	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL103	CPU DP2 AL103	RT101	LOWP2P3	0.0001 S	DP AL103	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL104	CPU DP2 AL104	RT101	LOWP2P3	0.0001 S	DP AL104	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL105	CPU DP2 AL105	RT101	LOWP2P3	0.0001 S	DP AL105	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL106	CPU DP2 AL106	RT101	LOWP2P3	0.0001 S	DP AL106	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL107	CPU DP2 AL107	RT101	LOWP2P3	0.0001 S	DP AL107	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL108	CPU DP2 AL108	RT101	LOWP2P3	0.0001 S	DP AL108	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL109	CPU DP2 AL109	RT101	LOWP2P3	0.0001 S	DP AL109	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL110	CPU DP2 AL110	RT101	LOWP2P3	0.0001 S	DP AL110	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL111	CPU DP2 AL111	RT101	LOWP2P3	0.0001 S	DP AL111	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL112	CPU DP2 AL112	RT101	LOWP2P3	0.0001 S	DP AL112	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL113	CPU DP2 AL113	RT101	LOWP2P3	0.0001 S	DP AL113	RT101	LOWP2P3	0.0001 S
-> CPU DP2 AL114	CPU DP2 AL114	RT101	LOWP2P3	0.0001 S	DP			



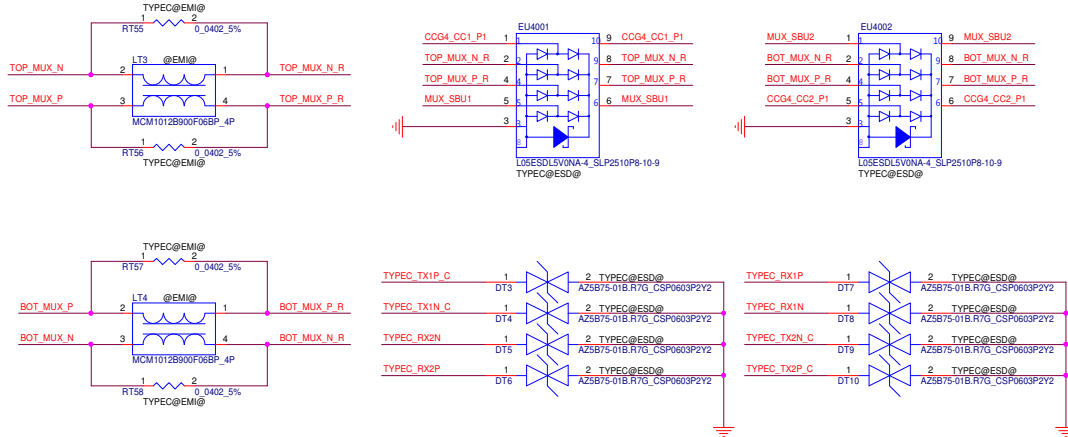
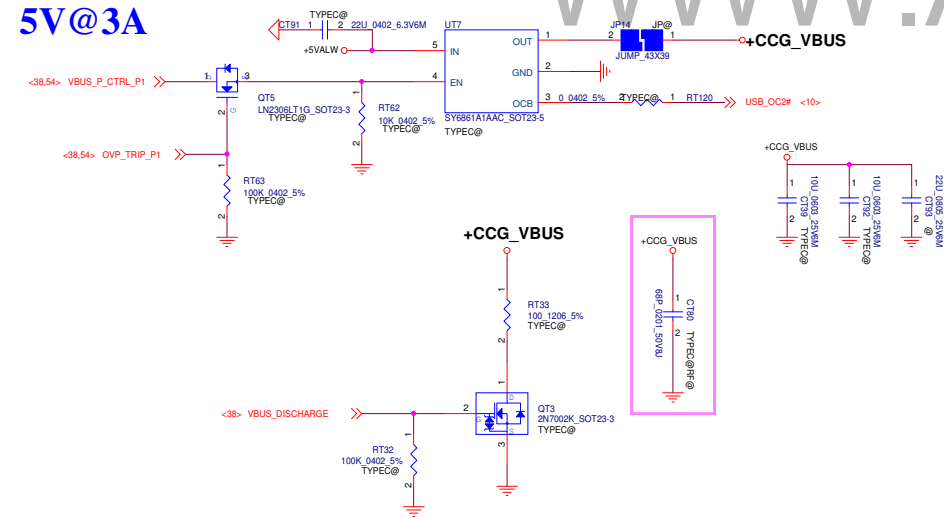
Close to JUSBC1 <500mil



MUX_USB2_FILP	MUX_A_EN	MUX_B_EN	A0_OUT	B0_OUT
0	0	1	--	USB2
0	1	1	I2C	USB2
1	1	0	USB2	--
1	1	1	USB2	I2C

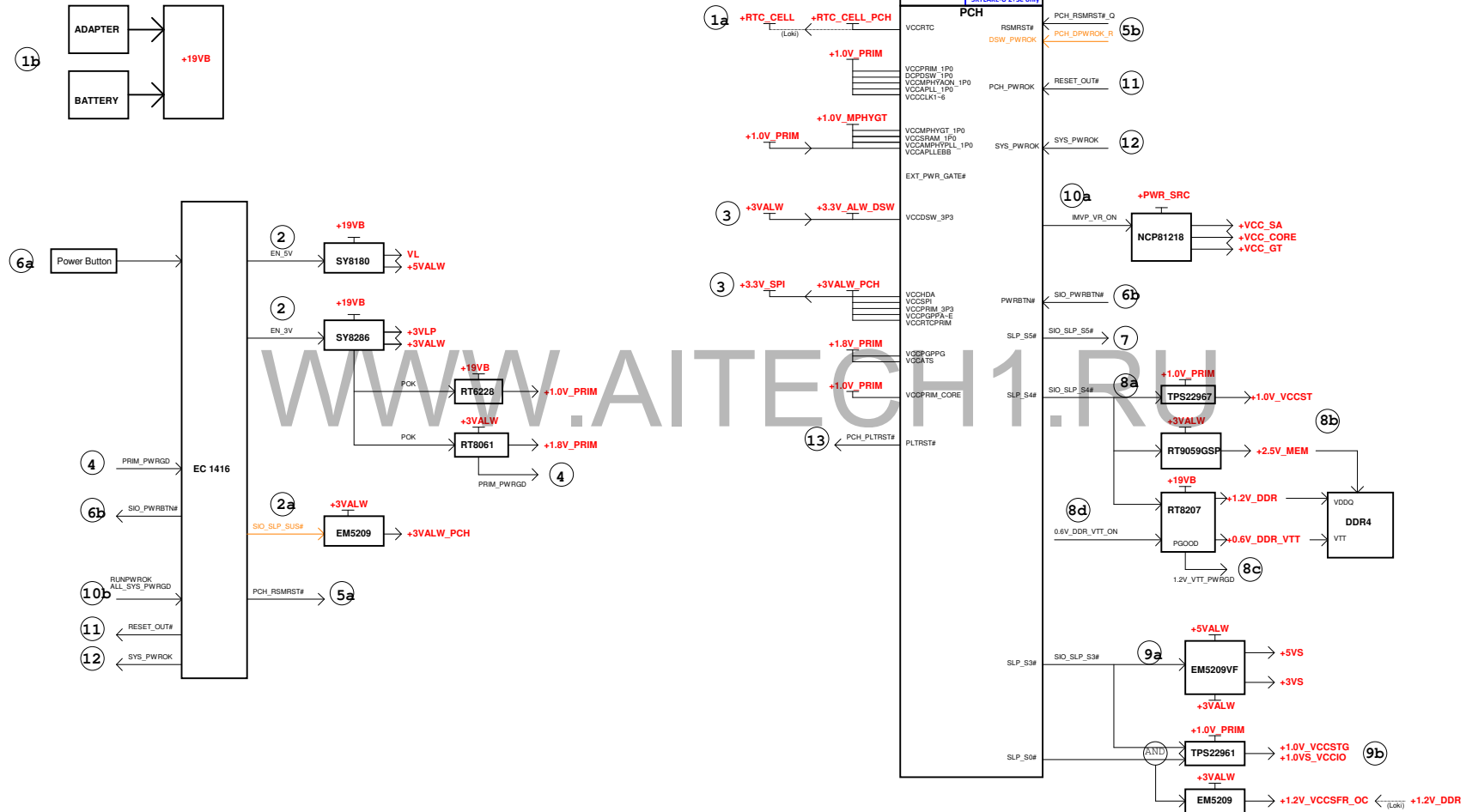


5V@3A



Type-C 5V Provide Path Control

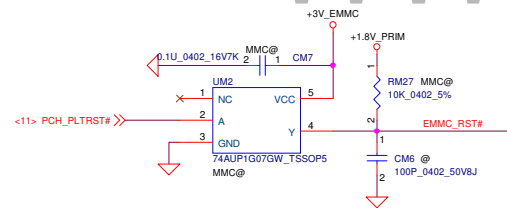
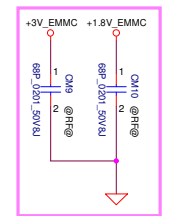
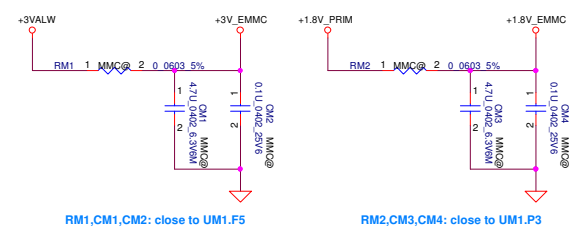
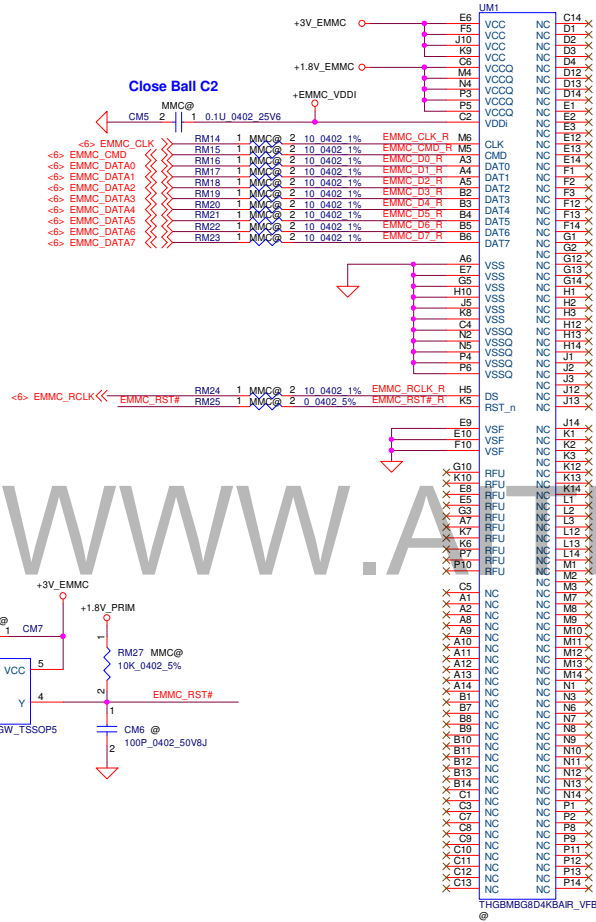
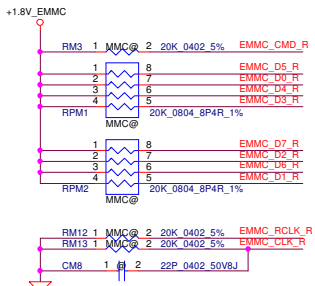
Timing Diagram for S5 to S0 mode



Security Classification	Compel Secret Data		 Compel Electronics, Inc.	
Issued Date	2016/12/01	Declassified Date	2017/12/01	 Platform Power Sequence
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<small>DATE</small> 2016/12/01 <small>DESIGN</small> 41 <small>OF</small> 05				

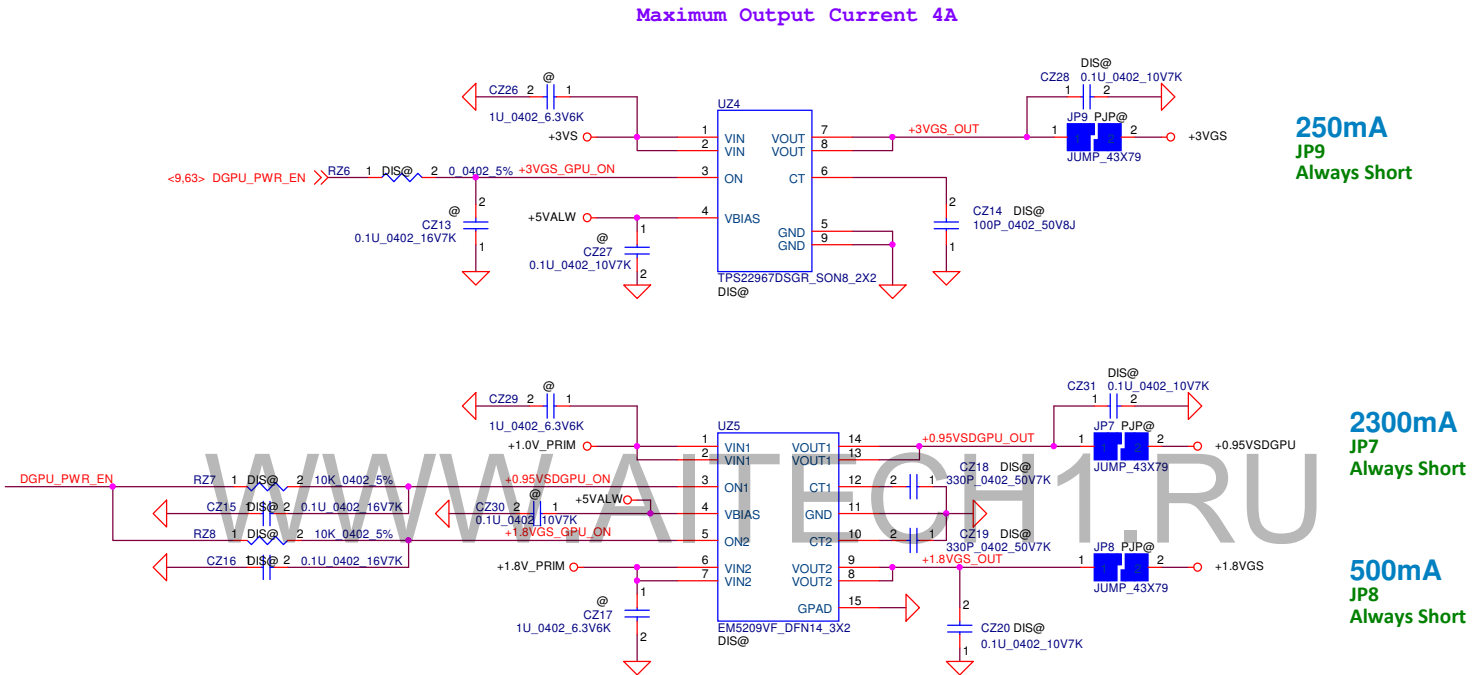
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Main Func = eMMC

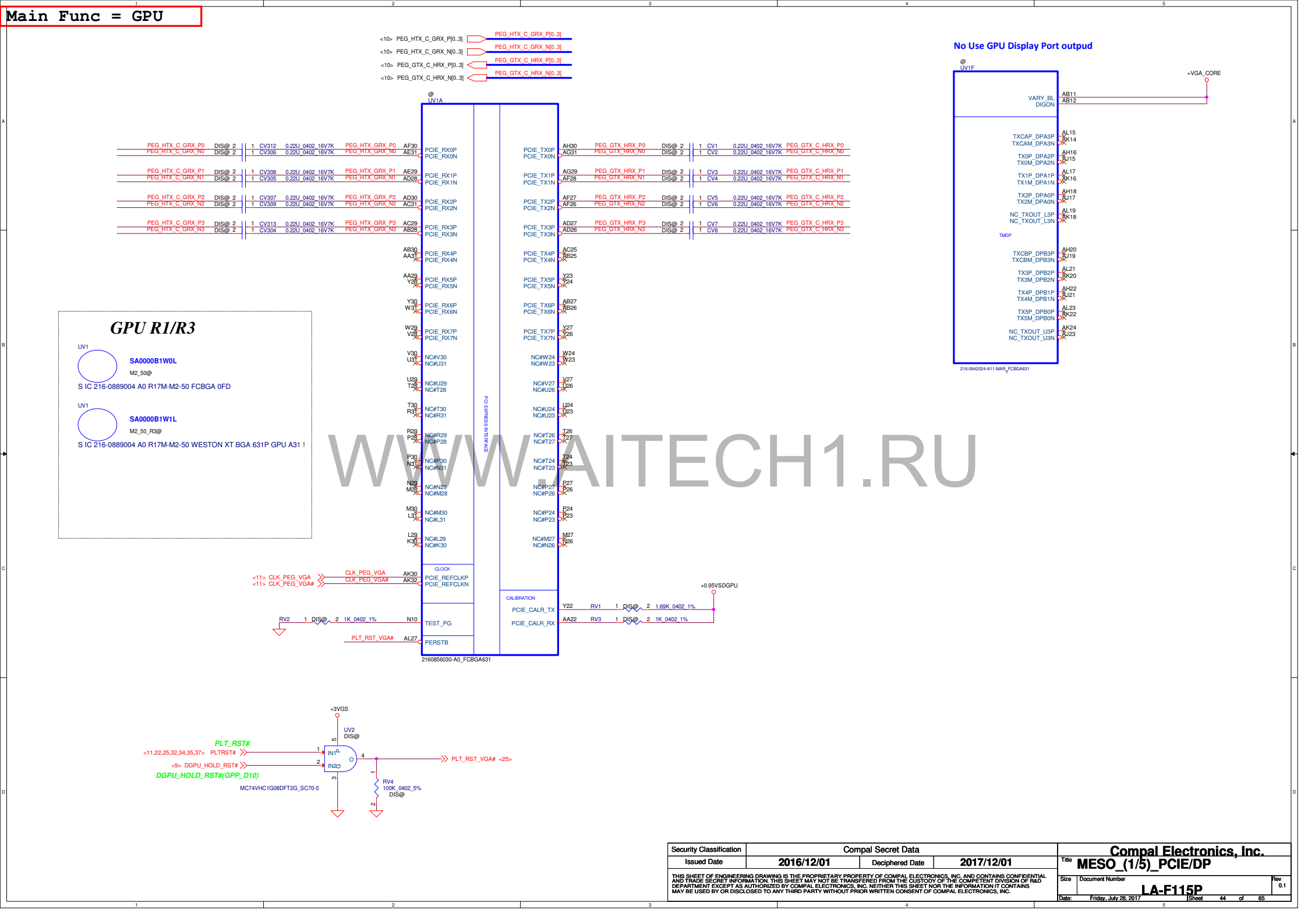


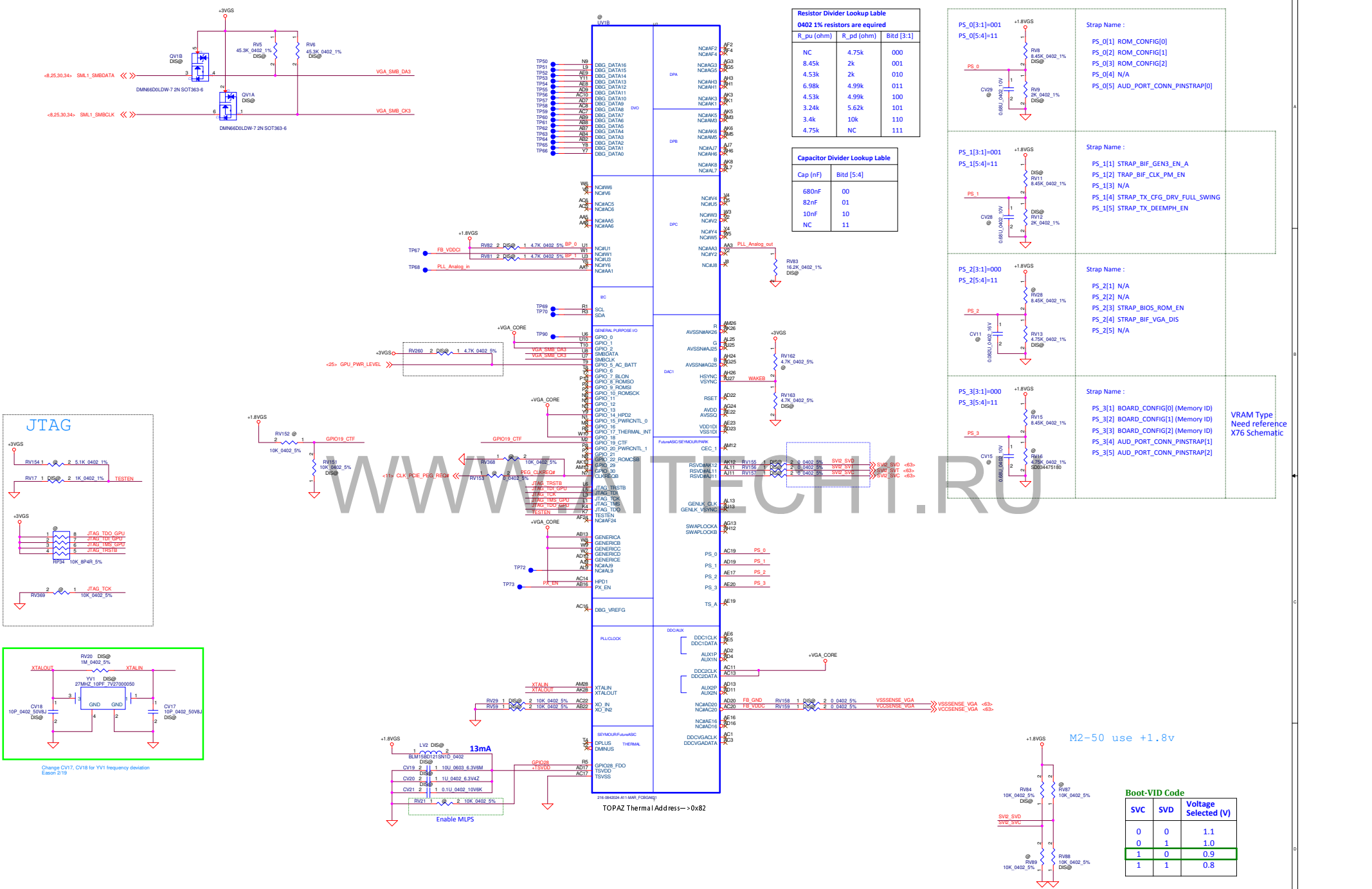
WWW.ATECH1.RU

+3V/+0.95V/+1.8V for GPU



Maximum Output Current 6A





Resistor Divider Lookup Table			
0402 1% resistors are required			
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]	
NC	4.75k	000	
8.45k	2k	001	
4.53k	2k	010	
6.98k	4.99k	011	
4.53k	4.99k	100	
3.24k	5.62k	101	
3.4k	10k	110	
4.75k	NC	111	

Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

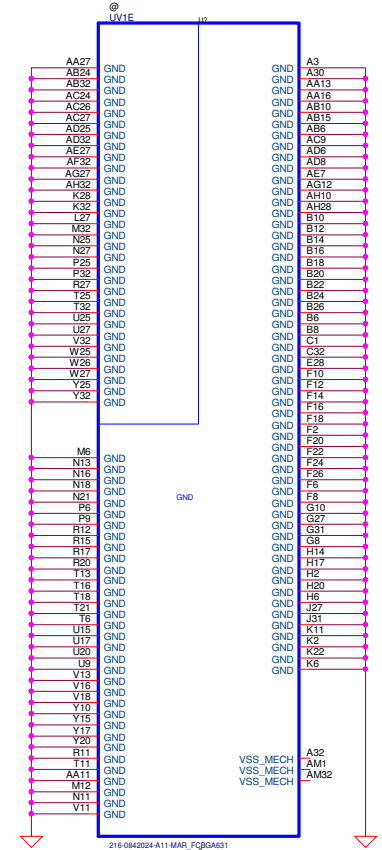
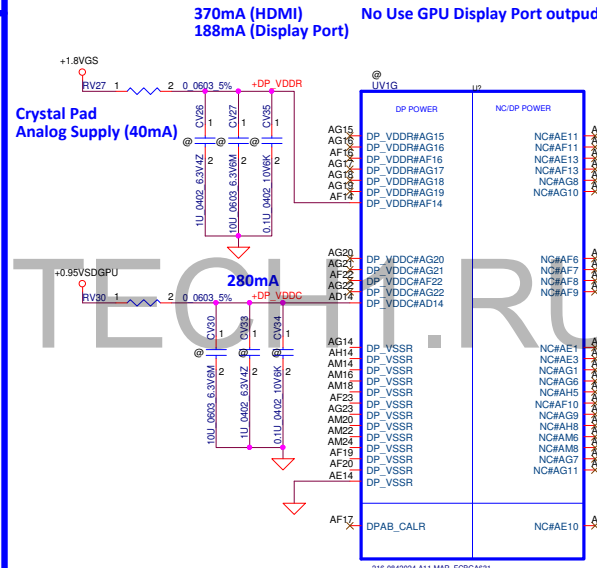
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	Strap Name : PS_1[1] STRAP_BIF_GEN3_EN_A PS_1[2] TRAP_BIF_CLK_PM_EN PS_1[3] N/A PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING PS_1[5] STRAP_TX_DEEMPH_EN
	Strap Name : PS_2[1] N/A PS_2[2] N/A PS_2[3] STRAP_BIOS_ROM_EN PS_2[4] STRAP_BIF_VGA_DIS PS_2[5] N/A
	Strap Name : PS_3[1] BOARD_CONFIG[0] (Memory ID) PS_3[2] BOARD_CONFIG[1] (Memory ID) PS_3[3] BOARD_CONFIG[2] (Memory ID) PS_3[4] AUD_PORT_CONN_PINSTRAP[1] PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

VRAM Type
Need reference
X76 Schematic

M2-50 use +1.8v

Boot-VID Code		
SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Main Func = GPU



Security Classification		Compal Secret Data		Compal Electronics, Inc. MESO (3/5) Power/GND	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title	
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				Date: Friday, July 28, 2017 Sheet 46 of 65	

Main Func = GPU

+VGA_CORE	10uF	1uF	0.1uF
VDDC	4	30	0
VDDCI	1	3	3

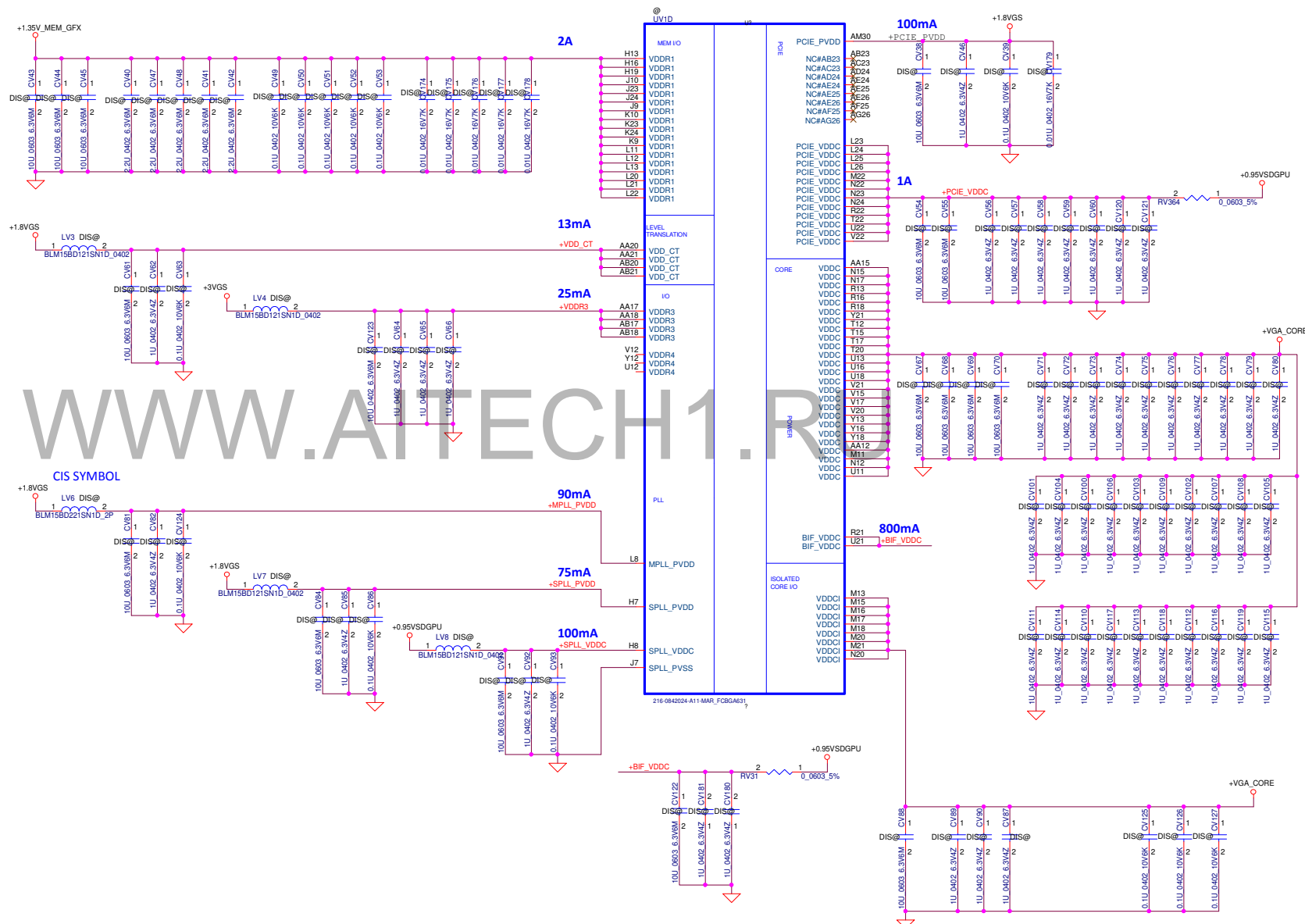
+0.95VSDGPU	10uF	1uF	0.1uF
PCIE_VDDC	2	7	0
BIF_VDDC	1	2	0
SPLL_VDDC	1	1	1
+DP_VDDC	0	0	0

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1	3	5	5	5

+1.8VGS	10uF	1uF	0.1uF
PCIE_PVDD	1	1	1
MPLL_PVDD	1	1	1
SPLL_PVDD	1	1	1

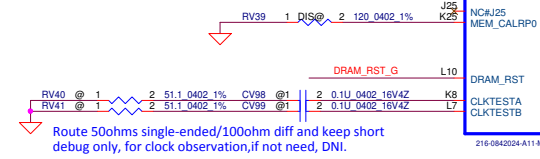
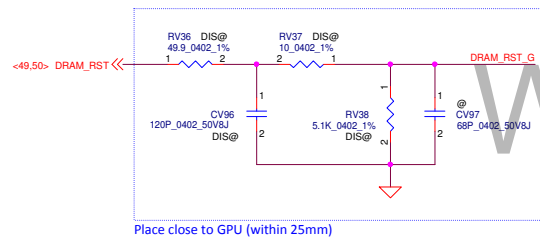
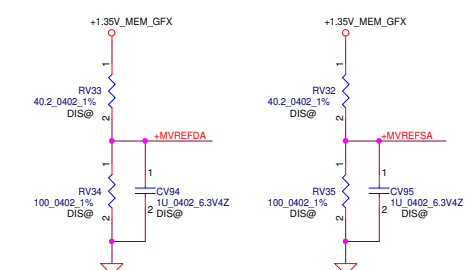
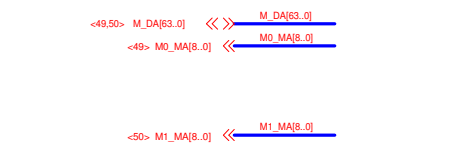
VDDR4 (NC)	0	0	0
VDD_CT	1	1	1
+TSVDD	1	1	1
+DP_VDDR	0	0	0

+3VGS	10uF	1uF	0.1uF
VDDR3	1	3	0



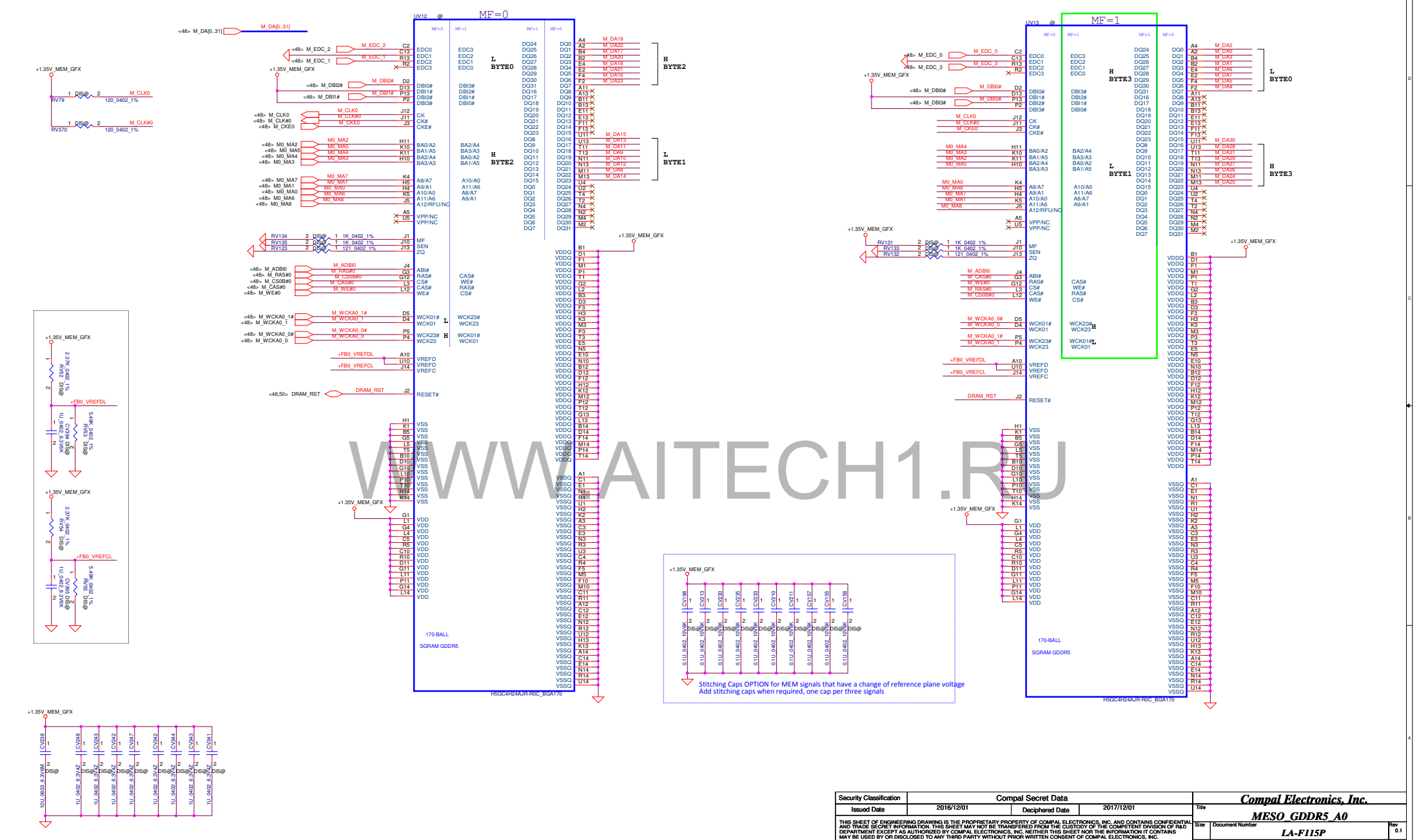
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title	MESO_(4/5)_Power
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				Custom	0.
Date: Friday, July 28, 2017				LA-F115P	
Sheet				47 of 65	

Main Func = GPU



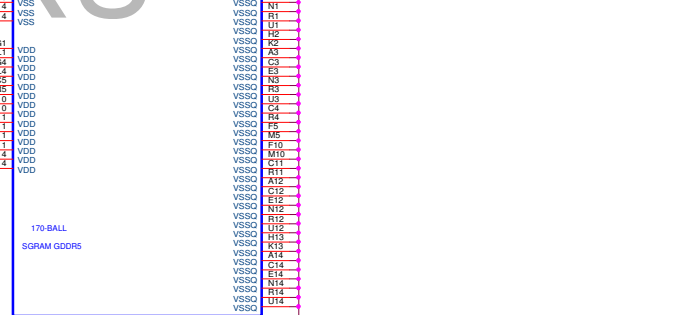
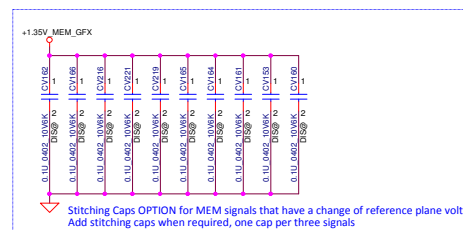
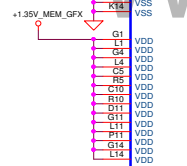
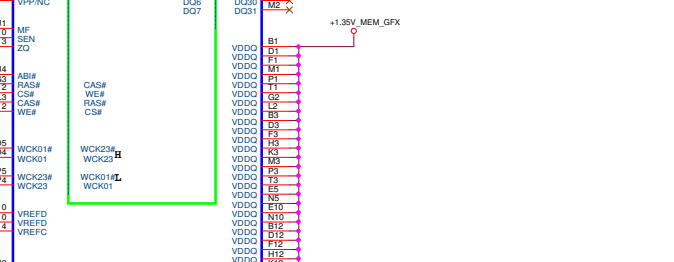
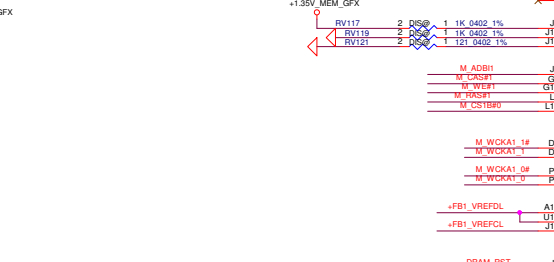
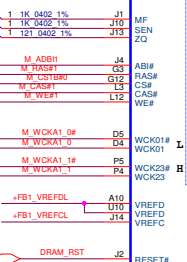
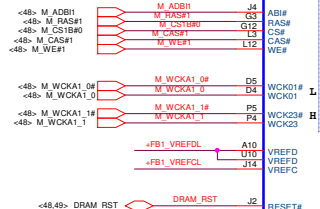
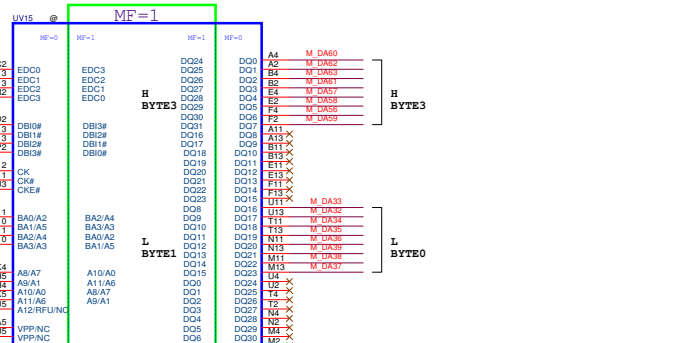
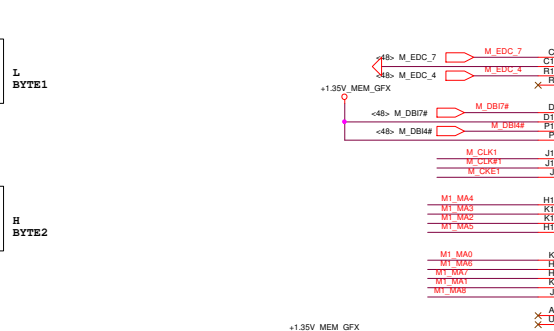
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M_DA1	J29	QDA0_1	MAA0_1/MAA_1	J20	M0_MAT
M_DA2	H30	QDA0_2	MAA0_2/MAA_2	H23	M0_MAZ
M_DA3	H32	QDA0_3	MAA0_3/MAA_3	G23	M0_MAS
M_DA4	G29	QDA0_4	MAA0_4/MAA_4	G24	M0_MAX
M_DA5	F28	QDA0_5	MAA0_5/MAA_5	H24	M0_MAS
M_DA6	F32	QDA0_6	MAA0_6/MAA_6	J18	M0_MAS
M_DA7	F30	QDA0_7	MAA0_7/MAA_7	K19	M0_MAY
M_DA8	C30	QDA0_8	MAA0_8/MAA_8	G20	M0_MAS
M_DA9	F27	QDA0_9	MAA0_9/MAA_9	L17	M0_MAS
M_DA10	A28	QDA0_10	MAA1_0/MAA_8	K	M1_MAO
M_DA11	C28	QDA0_11	MAA1_1/MAA_9	J14	M1_MAT
M_DA12	E27	QDA0_12	MAA1_2/MAA_10	J11	M1_MAZ
M_DA13	G26	QDA0_13	MAA1_3/MAA_11	J13	M1_MAS
M_DA14	D26	QDA0_14	MAA1_4/MAA_12	H11	M1_MAX
M_DA15	F25	QDA0_15	MAA1_5/MAA_BA2	G11	M1_MAS
M_DA16	A25	QDA0_16	MAA1_6/MAA_BA0	J18	M1_MAS
M_DA17	C25	QDA0_17	MAA1_7/MAA_BA1	L15	M1_MAY
M_DA18	E25	QDA0_18	MAA1_8/MAA_14	G14	M1_MAS
M_DA19	D24	QDA0_19	MAA1_9/RSVD	L16	M1_MAS
M_DA20	E23	QDA0_20	WCKA0_0/QDMA0_0	E32	M_WCKA0_0
M_DA21	F23	QDA0_21	WCKA0B_0/QDMA0_1	E30	M_WCKA0_0#
M_DA22	D22	QDA0_22	WCKA0_1/QDMA0_2	A21	M_WCKA0_1
M_DA23	F21	QDA0_23	WCKA0B_1/QDMA0_3	C21	M_WCKA0_1#
M_DA24	E21	QDA0_24	WCKA1_0/QDMA1_0	E13	M_WCKA1_0
M_DA25	D20	QDA0_25	WCKA1B_0/QDMA1_1	D12	M_WCKA1_0#
M_DA26	F19	QDA0_26	WCKA1_1/QDMA1_2	E3	M_WCKA1_1
M_DA27	A19	QDA0_27	WCKA1B_1/QDMA1_3	F4	M_WCKA1_1#
M_DA28	D18	QDA0_28	EDCA0_0/QSA0_0	H28	M_EDC_0
M_DA29	F17	QDA0_29	EDCA0_1/QSA0_1	C27	M_EDC_1
M_DA30	A17	QDA0_30	EDCA0_2/QSA0_2	A23	M_EDC_2
M_DA31	C17	QDA0_31	EDCA0_3/QSA0_3	E19	M_EDC_3
M_DA32	E17	QDA1_0	EDCA1_0/QSA1_0	E18	M_EDC_4
M_DA33	D16	QDA1_1	EDCA1_1/QSA1_1	D10	M_EDC_5
M_DA34	F15	QDA1_2	EDCA1_2/QSA1_2	D6	M_EDC_6
M_DA35	D14	QDA1_3	EDCA1_3/QSA1_3	G5	M_EDC_7
M_DA36	F13	QDA1_4	DBIA0_0/QSA0_0B	A27	M_DBI0#
M_DA37	A13	QDA1_5	DBIA0_1/QSA0_1B	A27	M_DBI1#
M_DA38	C13	QDA1_6	DBIA0_2/QSA0_2B	G23	M_DBI2#
M_DA39	E11	QDA1_7	DBIA0_3/QSA0_3B	G15	M_DBI3#
M_DA40	A11	QDA1_8	DBIA1_0/QSA1_0B	E9	M_DBI4#
M_DA41	C11	QDA1_9	DBIA1_1/QSA1_1B	G5	M_DBI5#
M_DA42	F11	QDA1_10	DBIA1_2/QSA1_2B	H4	M_DBI6#
M_DA43	A9	QDA1_11	DBIA1_3/QSA1_3B	L18	M_ADBI0
M_DA44	C9	QDA1_12	ADBI0/ODTA0	K16	M_ADBI1
M_DA45	E9	QDA1_13	ADBI1/ODTA1	H26	M_CLK0
M_DA46	F9	QDA1_14	CLKA0	H25	M_CLK0#
M_DA47	D8	QDA1_15	CLKA1	G8	M_CLK1
M_DA48	E7	QDA1_16	CLKA1B	H9	M_CLK1#
M_DA49	A7	QDA1_17	RASA0B	G22	M_RAS#0
M_DA50	C7	QDA1_18	RASA1B	G17	M_RAS#1
M_DA51	E7	QDA1_19	CASA0B	G19	M_CAS#0
M_DA52	A5	QDA1_20	CASA1B	G16	M_CAS#1
M_DA53	E5	QDA1_21	CSA0B_0	H22	M_CS0B#0
M_DA54	C3	QDA1_22	CSA0B_1	J22	M_CS1B#0
M_DA55	E1	QDA1_23	CSA1B_0	G13	M_CS1B#0
M_DA56	G7	QDA1_24	CSA1B_1	K13	M_CKE0
M_DA57	G6	QDA1_25	CKEA0	K20	M_CKE1
M_DA58	G1	QDA1_26	CKEA1	J17	M_WE#0
M_DA59	G3	QDA1_27	WEA0B	G25	M_WE#1
M_DA60	J6	QDA1_28	WEA1B	H10	M_WE#1
M_DA61	J1	QDA1_29			
M_DA62	J5	QDA1_30			
M_DA63	J5	QDA1_31			
+MVREFDA	K26	MVREFDA			
+MVREFSA	J26	MVREFSA			
NCU25	J25	MEM_CALRPO			
DRAM_RST_G	L10	DRAM_RST			
CLKTESTA	K8	CLKTESTA			
CLKTESTB	L7	CLKTESTB			

Main Func = GDDR5



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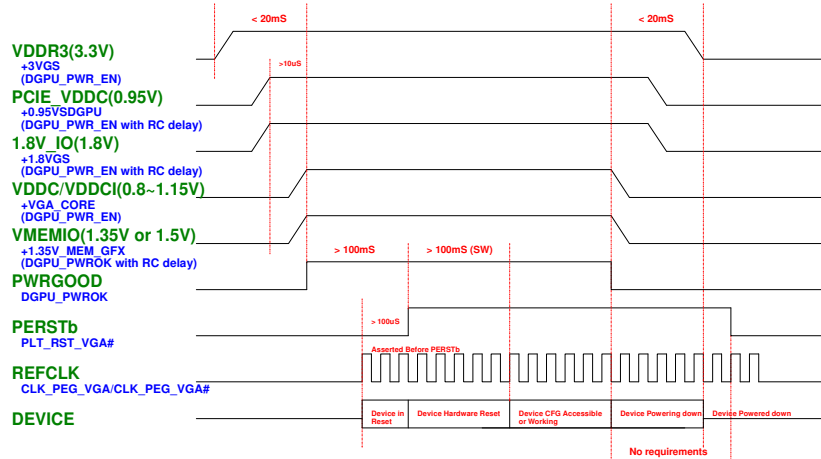


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				Rev 0.1
Date:	Enforce Date: 98-10-17	Expiry:	50	of 65

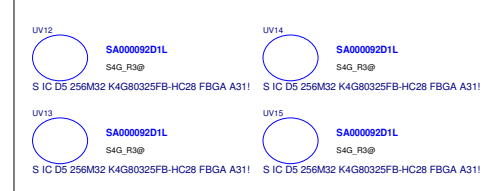
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

AMD PowerXpress® idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as 7.50 mV/ μ s). For power down, reversing the ramp-up sequence is recommended.



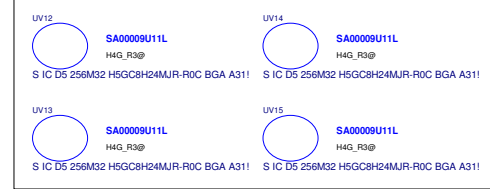
samsung 4G



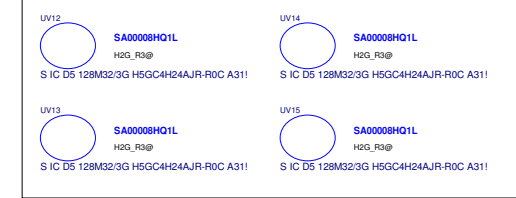
samsung 2G



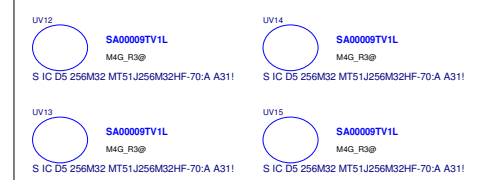
Hynix 4G



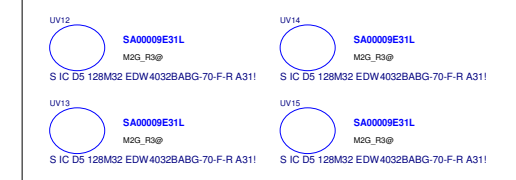
Hynix 2G



Micron 4G



Micron 2G



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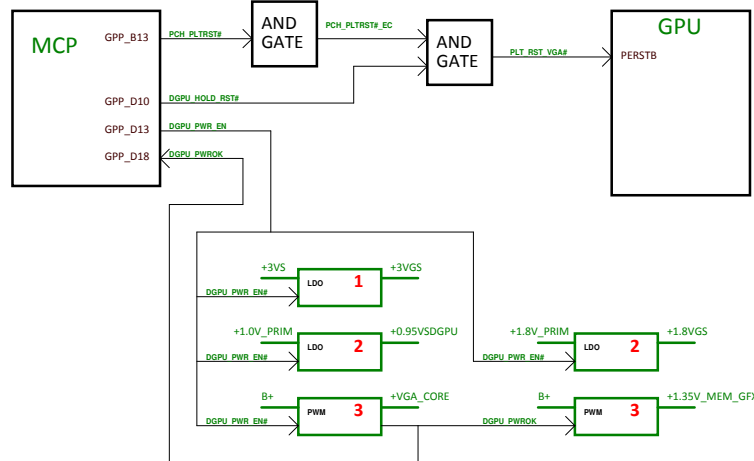


Table 3-21 Resistor Divider Lookup T.

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R17M-M2-50 VRAM Only

Memory ID	4Gb R3 P/N	Vendor	Configuration	Size
000	SA00009TT1L	SAMSUNG	S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	2GB
110	SA00008HQ1L	Hynix	S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	2GB
111	SA00009E31L	Micron	S IC D5 128M32 EDW4032BAGB-70-F-R A31!	2GB

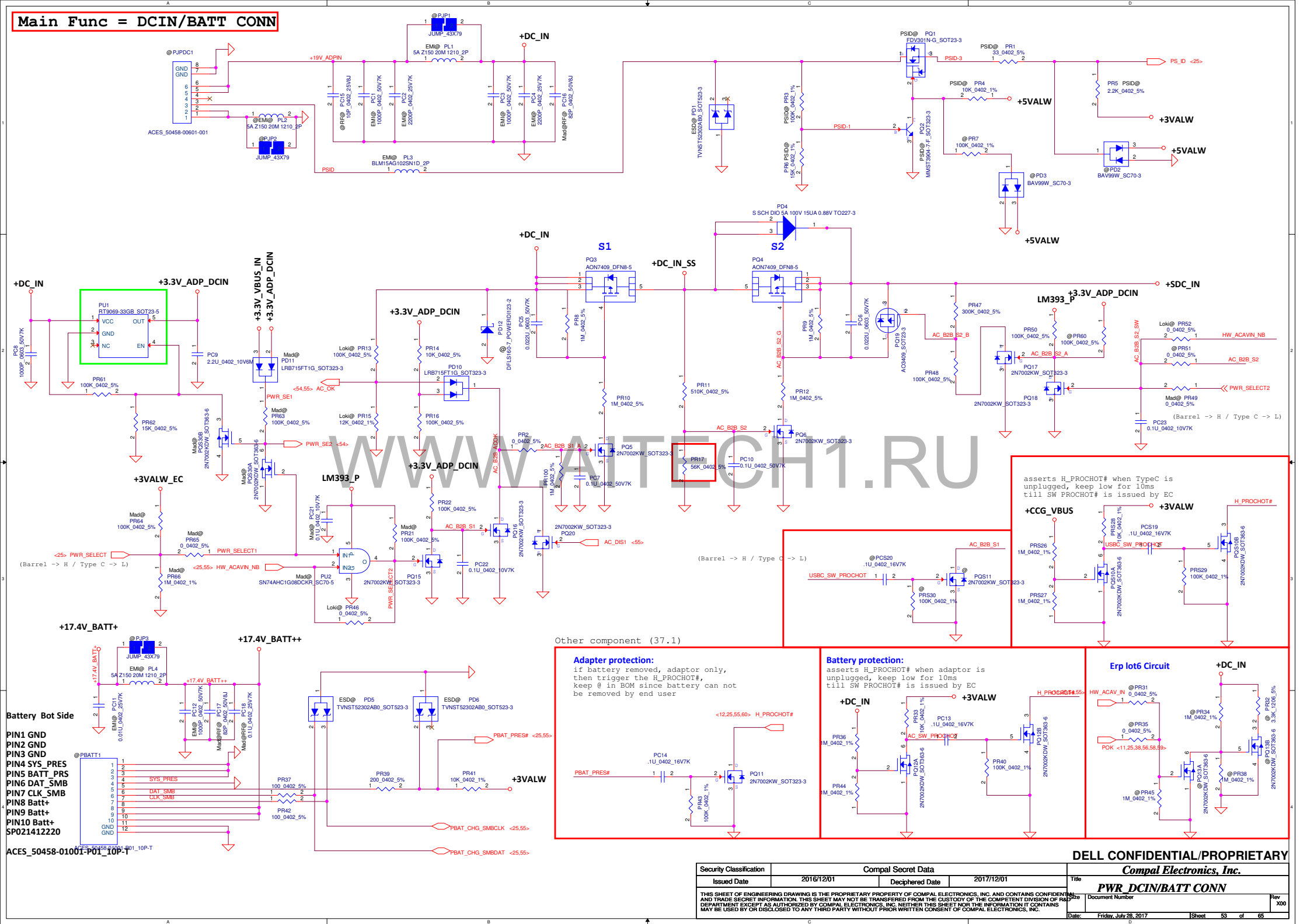
Memory ID	8Gb R3 P/N	Vendor	Configuration	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	4GB
110	SA00009U11L	Hynix	S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	4GB
111	SA00009TV1L	Micron	S IC D5 256M32 MT51J256M32HF-70-A A31!	4GB

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Main Func = DCIN/BATT CONN



Other component (37.1)

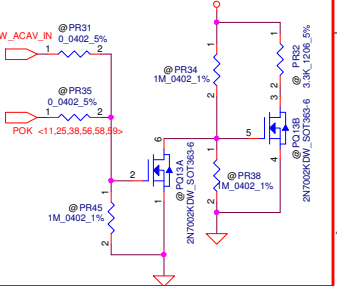
Adapter protection:

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep 0 in BOM since battery can not be removed by end user

Battery protection:

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC

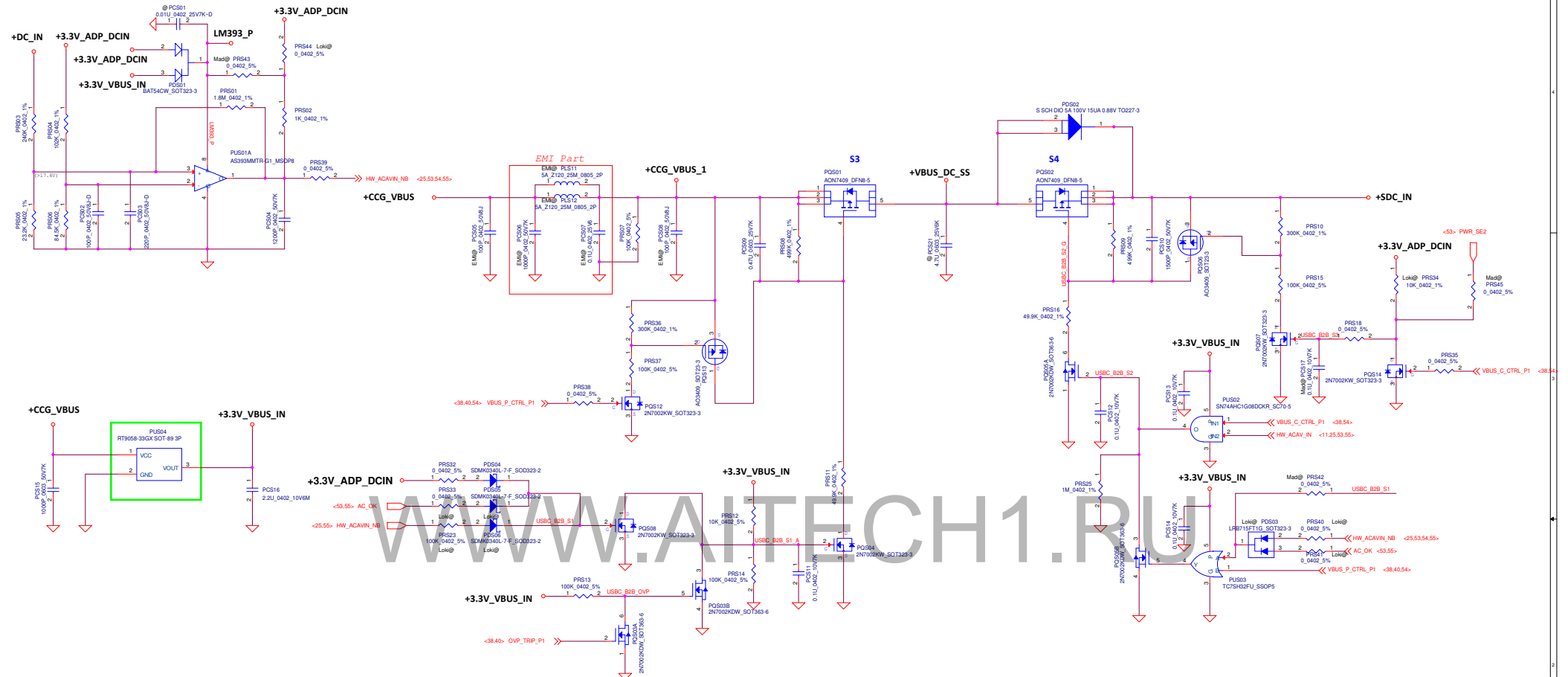
Erp lot6 Circuit



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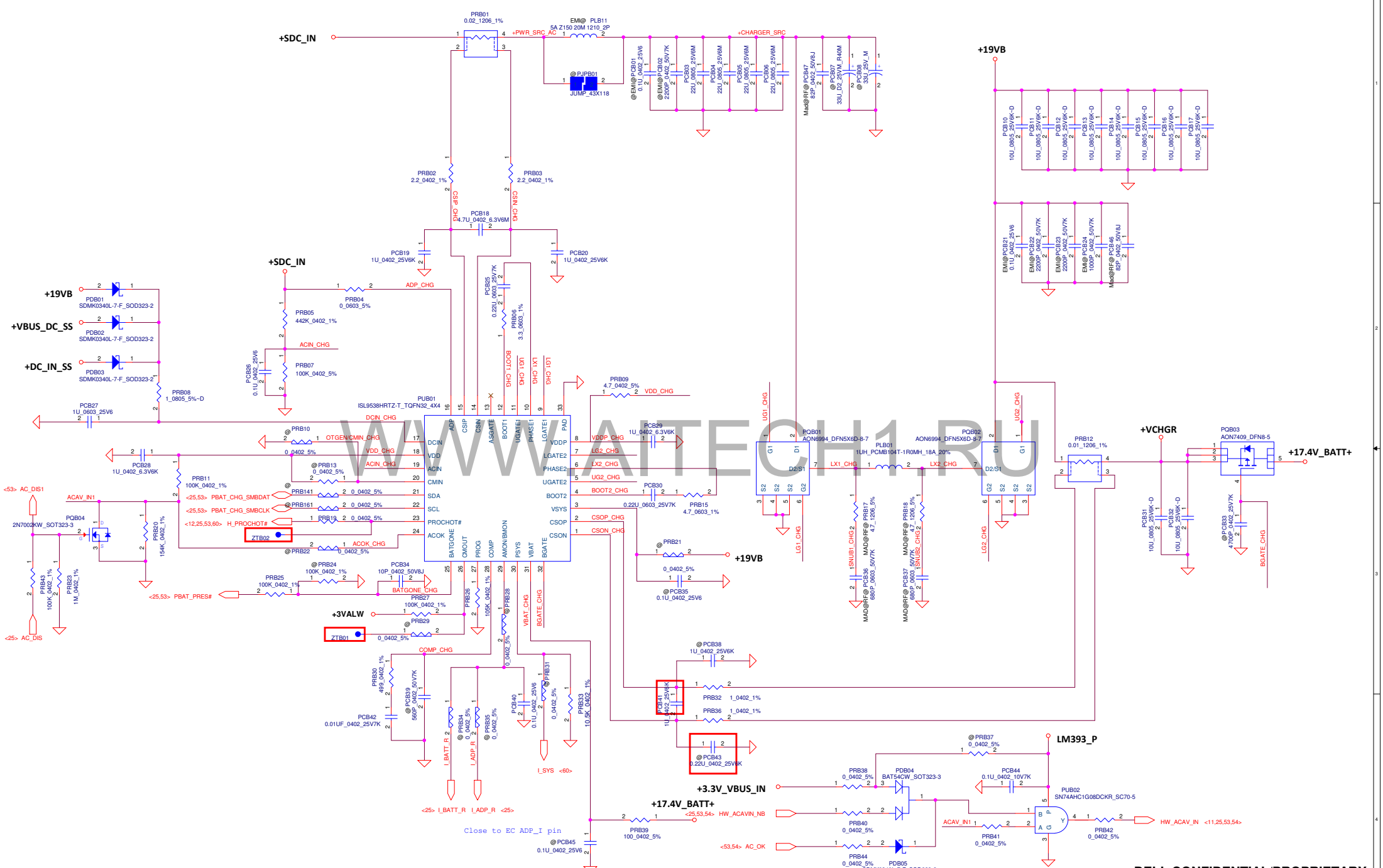
Main Func = Type-C PD Selector

DCIN_AC_Detector

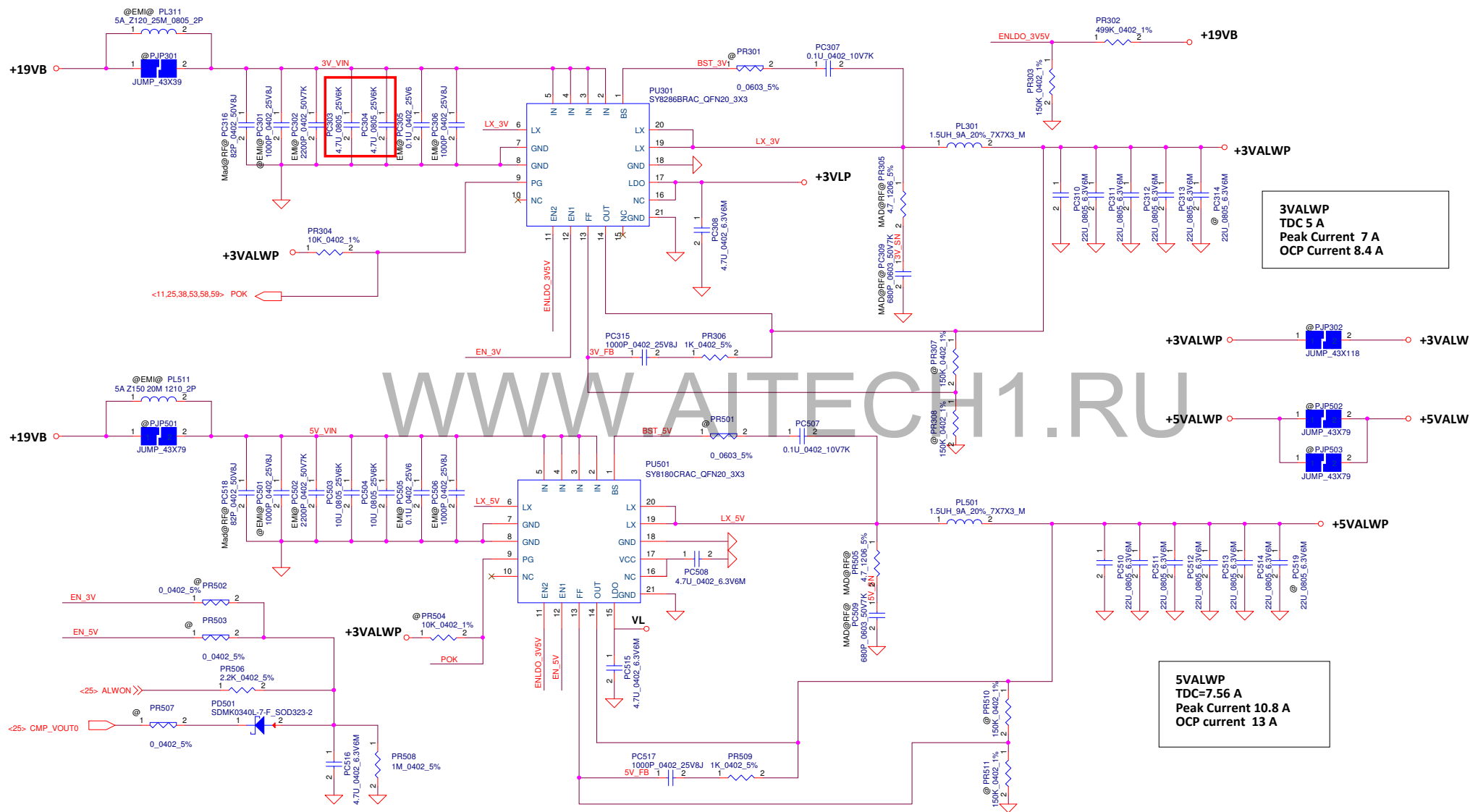


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Main Func = CHARGER

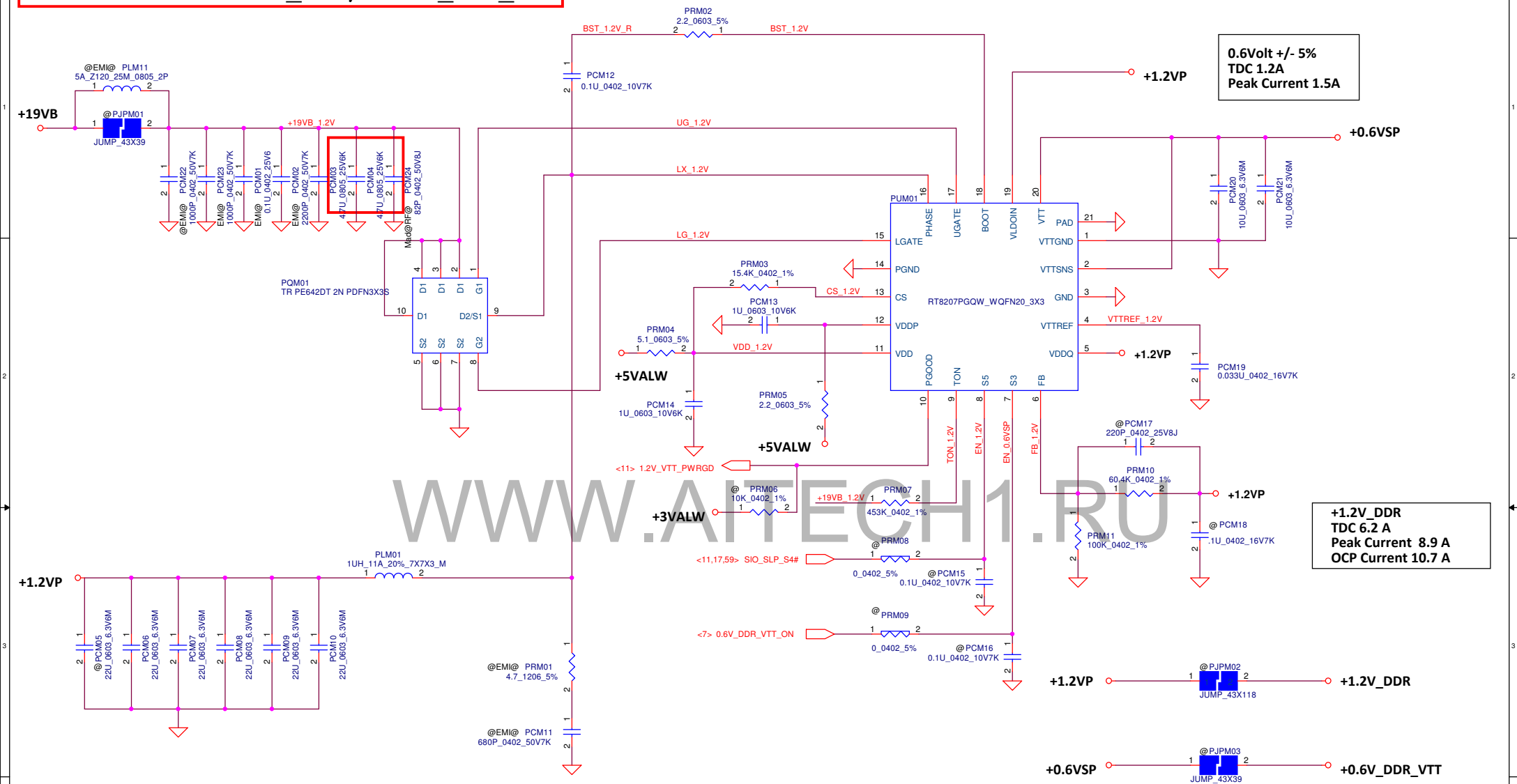


Main Func = 3.3VALWP/5VALWP



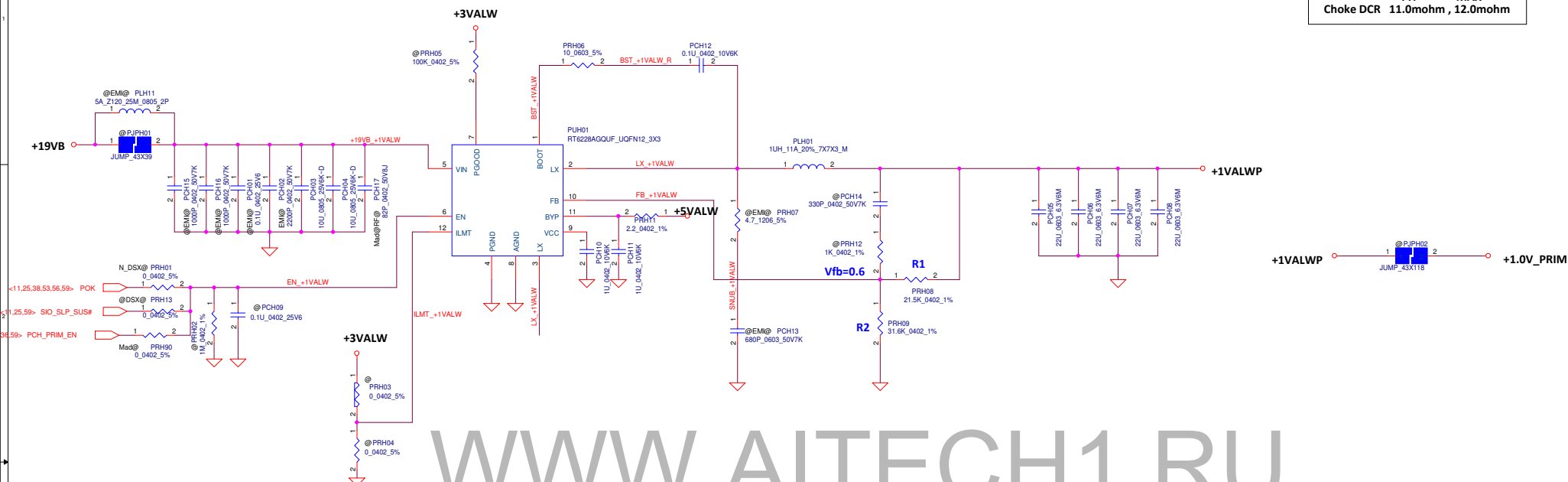
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Main Func = +1.2V_DDR/+0.6V_DDR_VTT



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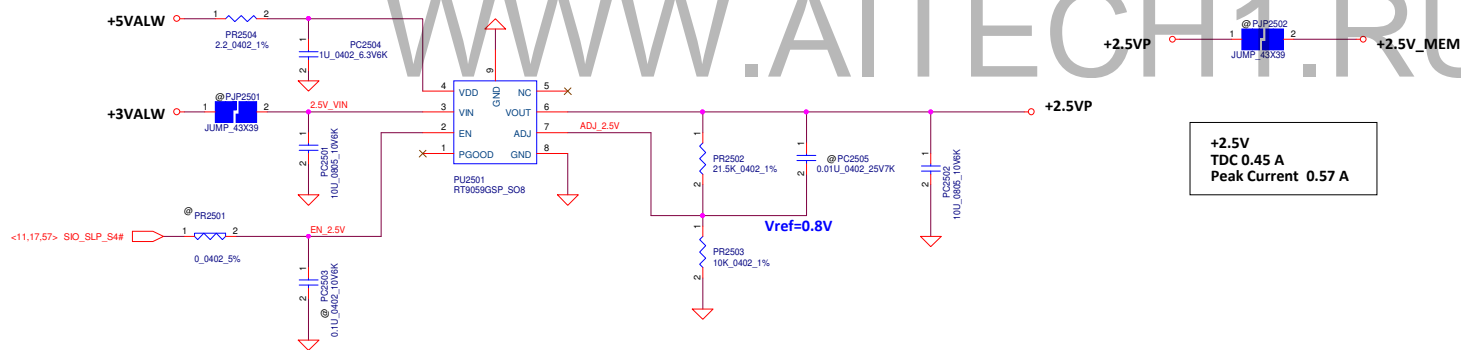
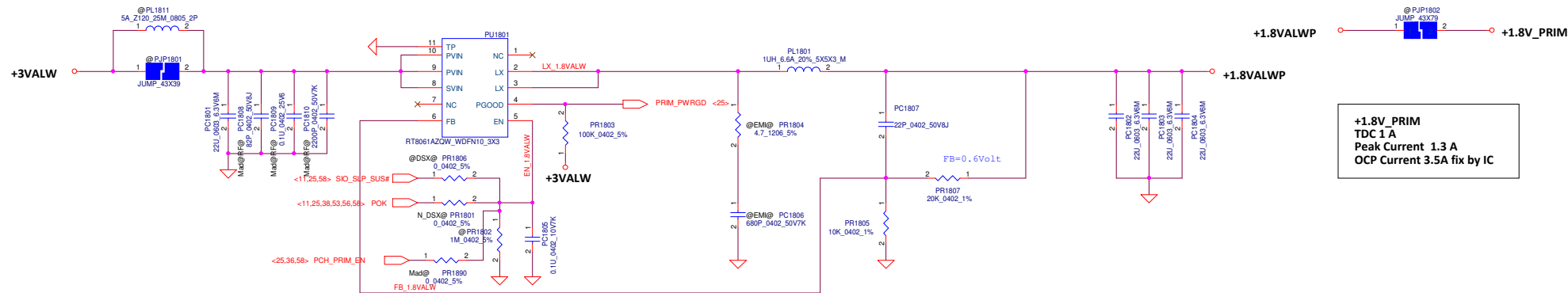
+1.0V_PRIM
TDC 7.6 A
Peak Current 10.8 A
OCP Current 12 A Fix by IC
Choke DCR 11.0mohm , 12.0mohm



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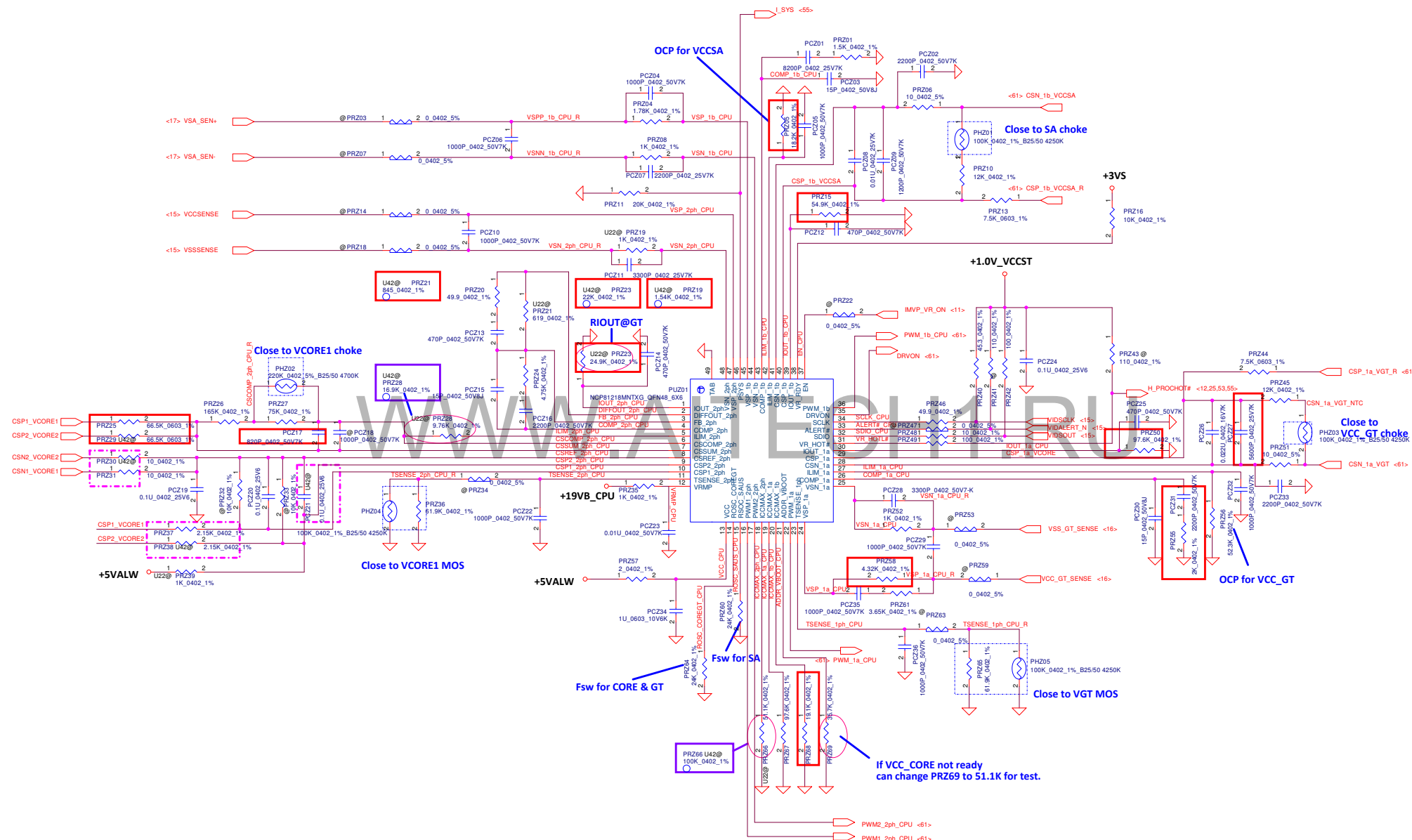
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Main Func = +1.8VALWP / +2.5VP



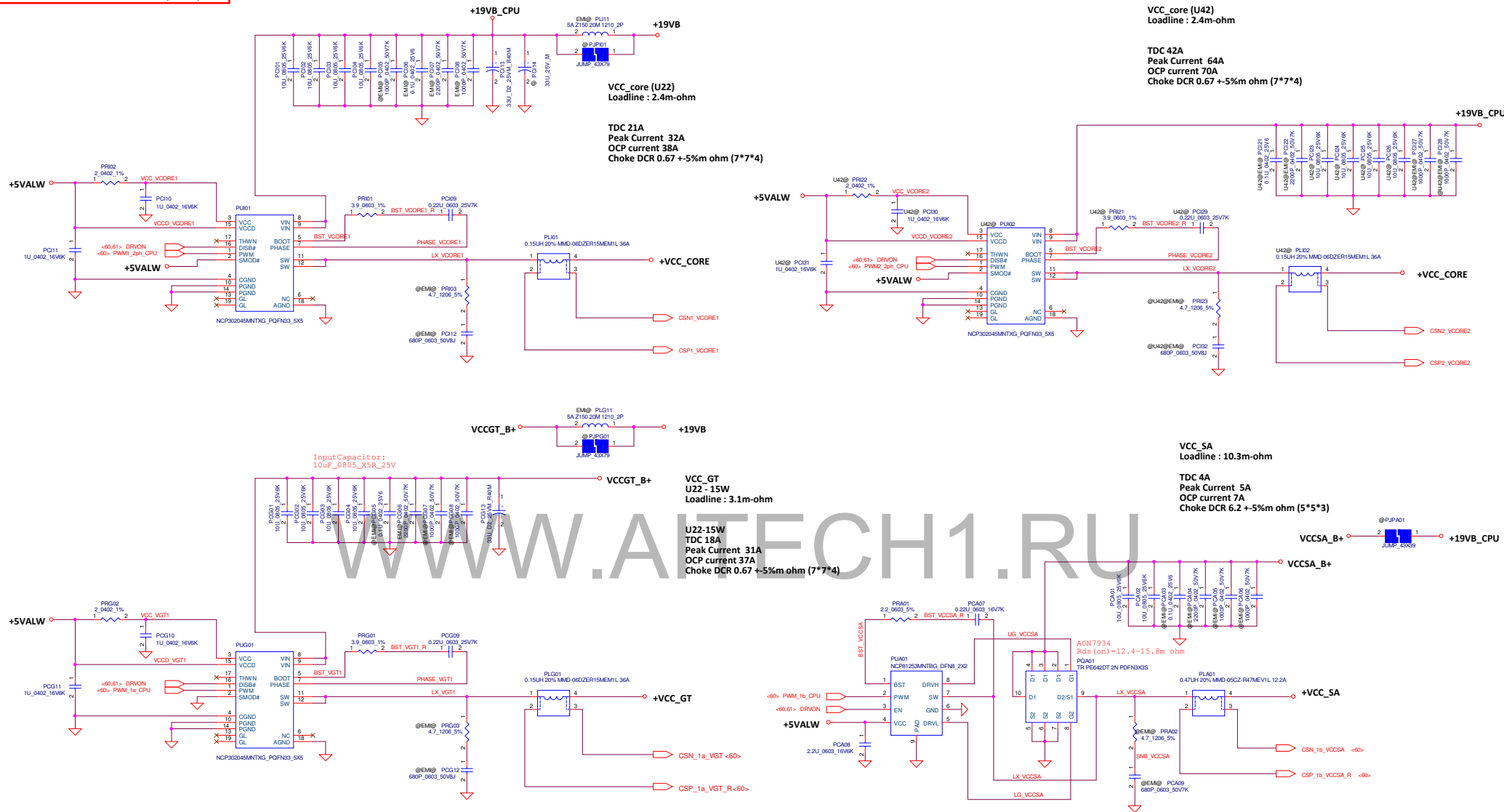
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Main Func = CPU



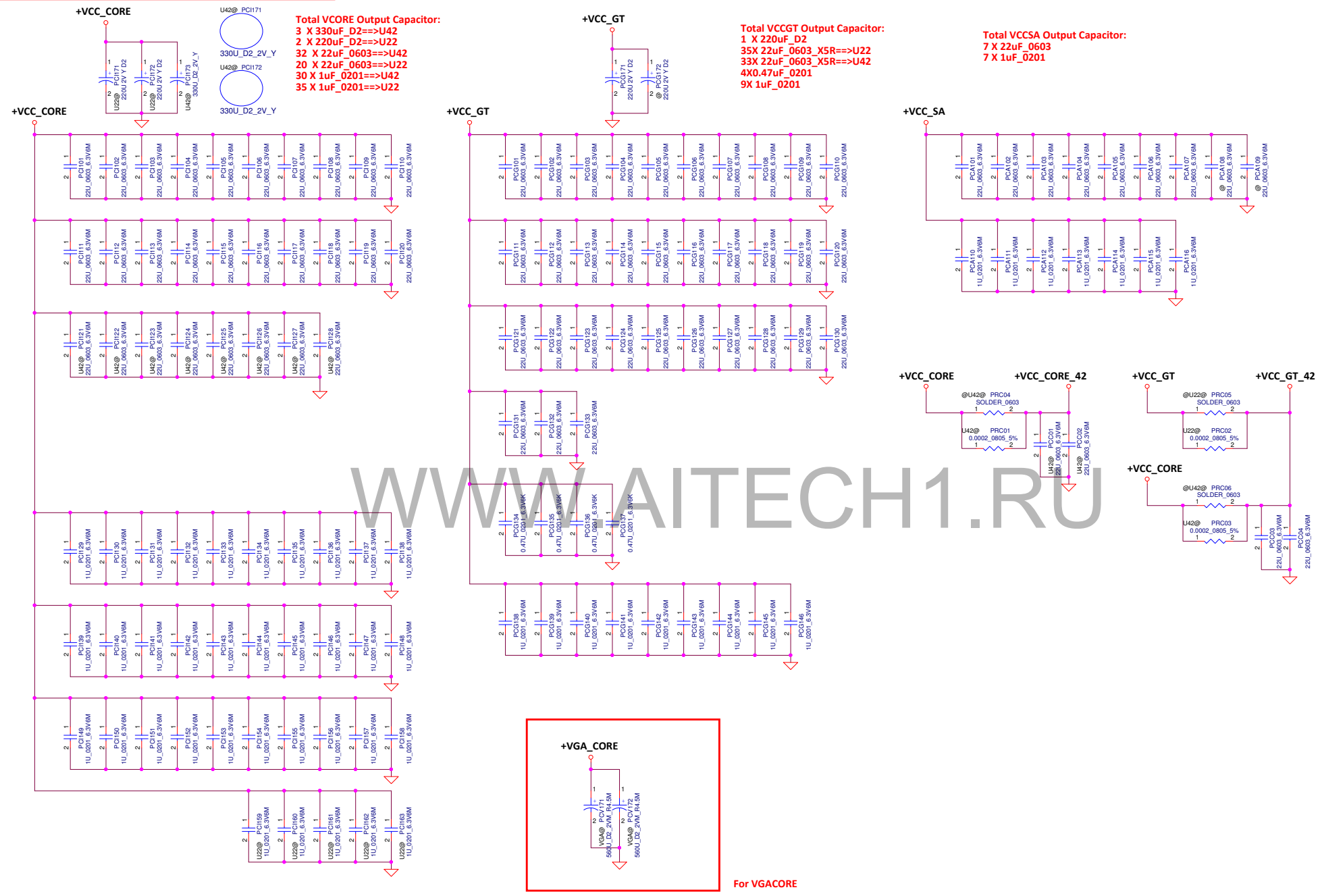
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Main Func = CPUcore IA/GT/SA

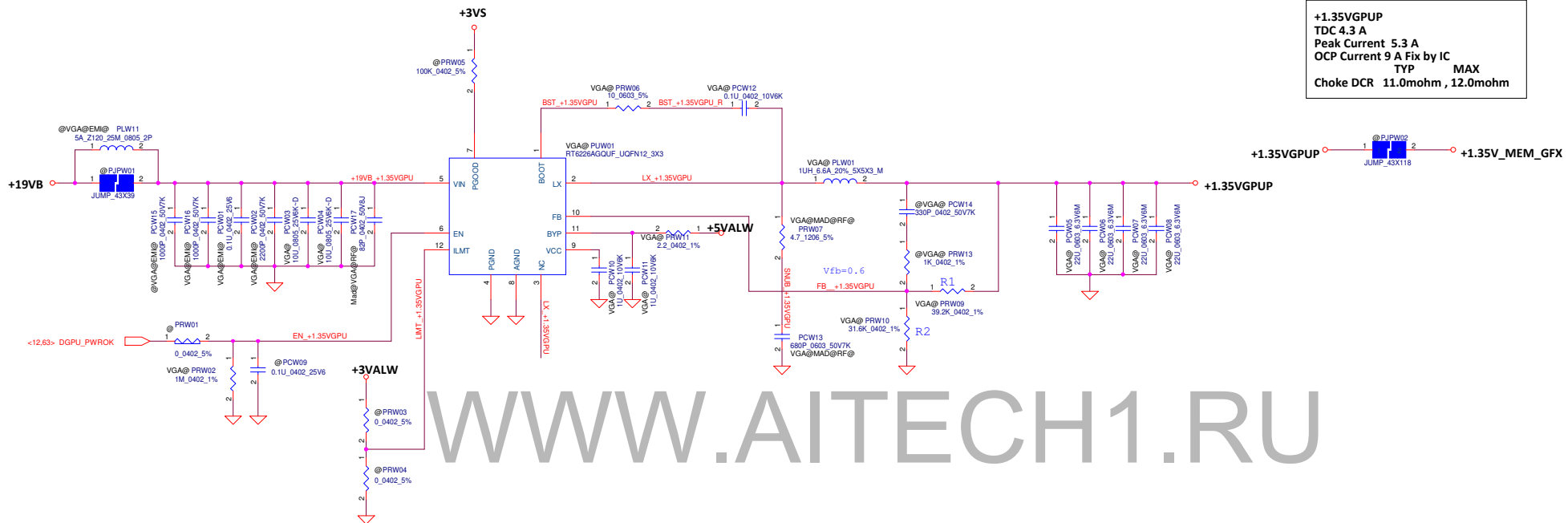


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Main Func = CPU/ VGA / SA MLCC



Main Func = +1.35VG PUP



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2	P56	PWR	20160321	COMPAL			0.1 (x00)
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